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Darwish et al.

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(54) **TRENCH MIS DEVICE WITH REDUCED GATE-TO-DRAIN CAPACITANCE**

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(51) **Int. Cl.**[7] **H01L 27/108**; H01L 29/76; H01L 29/94; H01L 31/119

(52) **U.S. Cl.** **257/307**; 257/302; 257/303; 257/304; 438/242; 438/243; 438/244

(58) **Field of Search** 257/301, 302, 257/303, 304; 438/242, 243, 244

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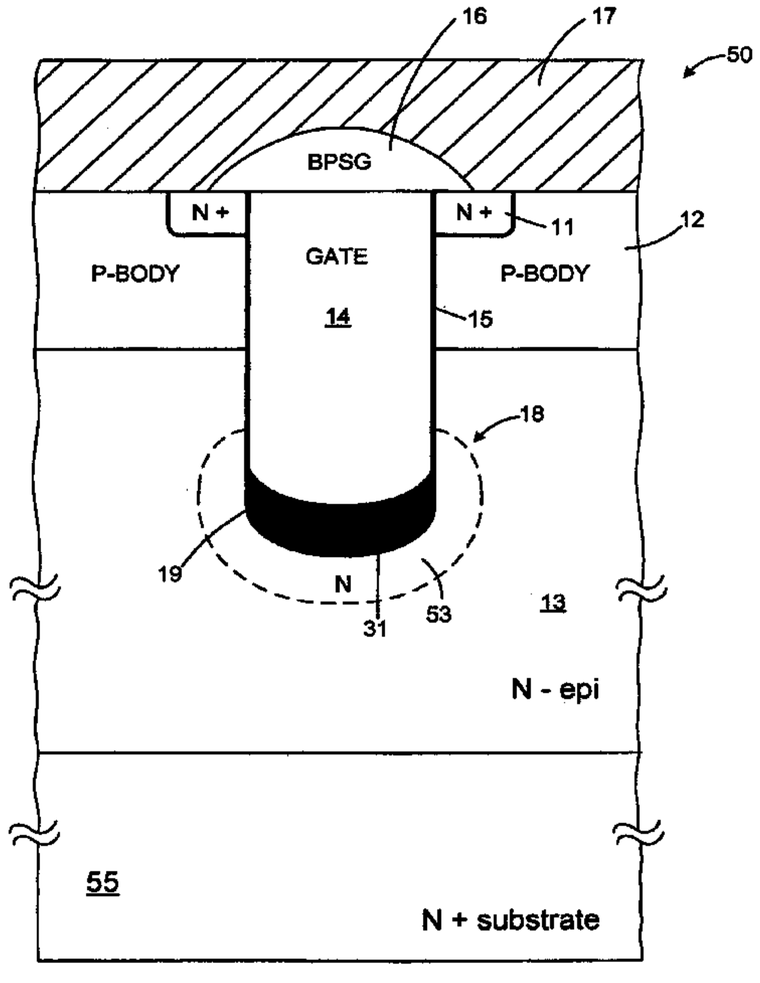
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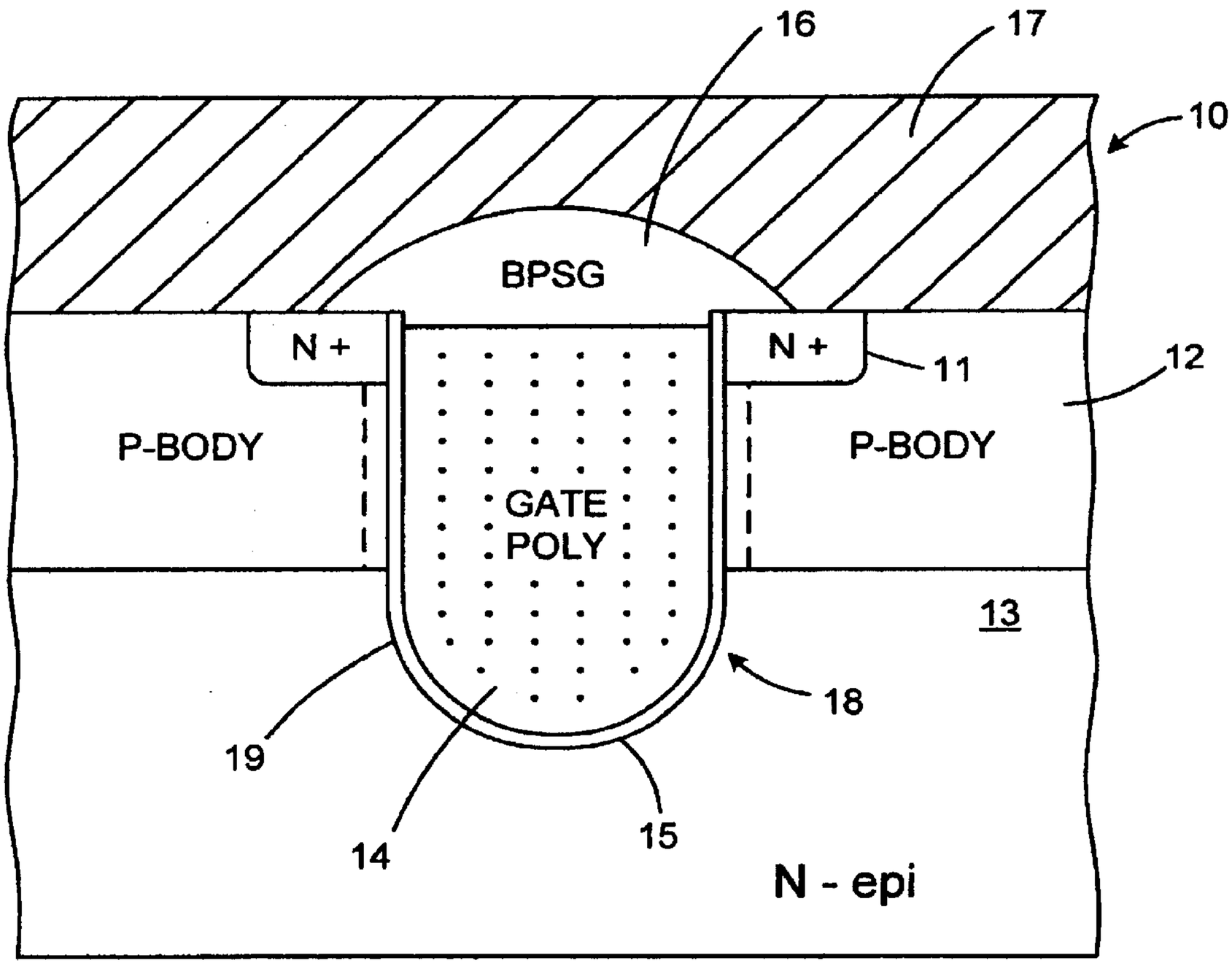
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(57) **ABSTRACT**

Trench MIS devices including a thick insulative layer at the bottom of the trench are disclosed, along with methods of fabricating such devices. An exemplary trench MOSFET embodiment includes a thick oxide layer at the bottom of the trench, with no appreciable change in stress in the substrate along the trench bottom. The thick insulative layer separates the trench gate from the drain region at the bottom of the trench yielding a reduced gate-to-drain capacitance making such MOSFETs suitable for high frequency applications. In an exemplary fabrication process embodiment, the thick insulative layer is deposited on the bottom of the trench. A thin insulative gate dielectric is formed on the exposed sidewall and is coupled to the thick insulative layer. A gate is formed in the remaining trench volume. The process is completed with body and source implants, passivation, and metallization.

19 Claims, 15 Drawing Sheets





PRIOR ART

FIG. 1

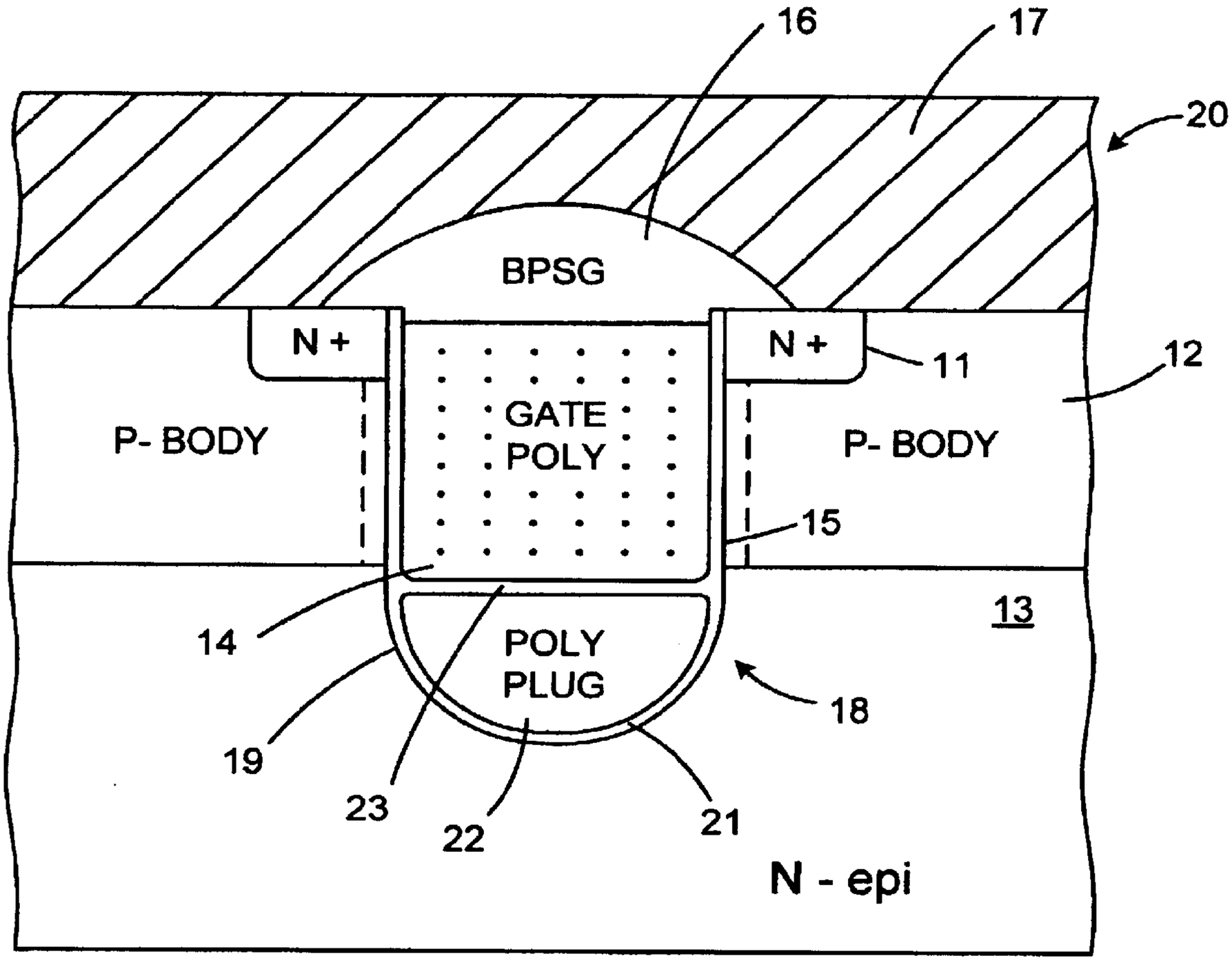

16
17
20
BPSG
N +
N +
11
12
GATE
POLY
P- BODY
P- BODY
15
13
14
POLY
PLUG
18
19
23
22
21
N - epi

FIG. 2

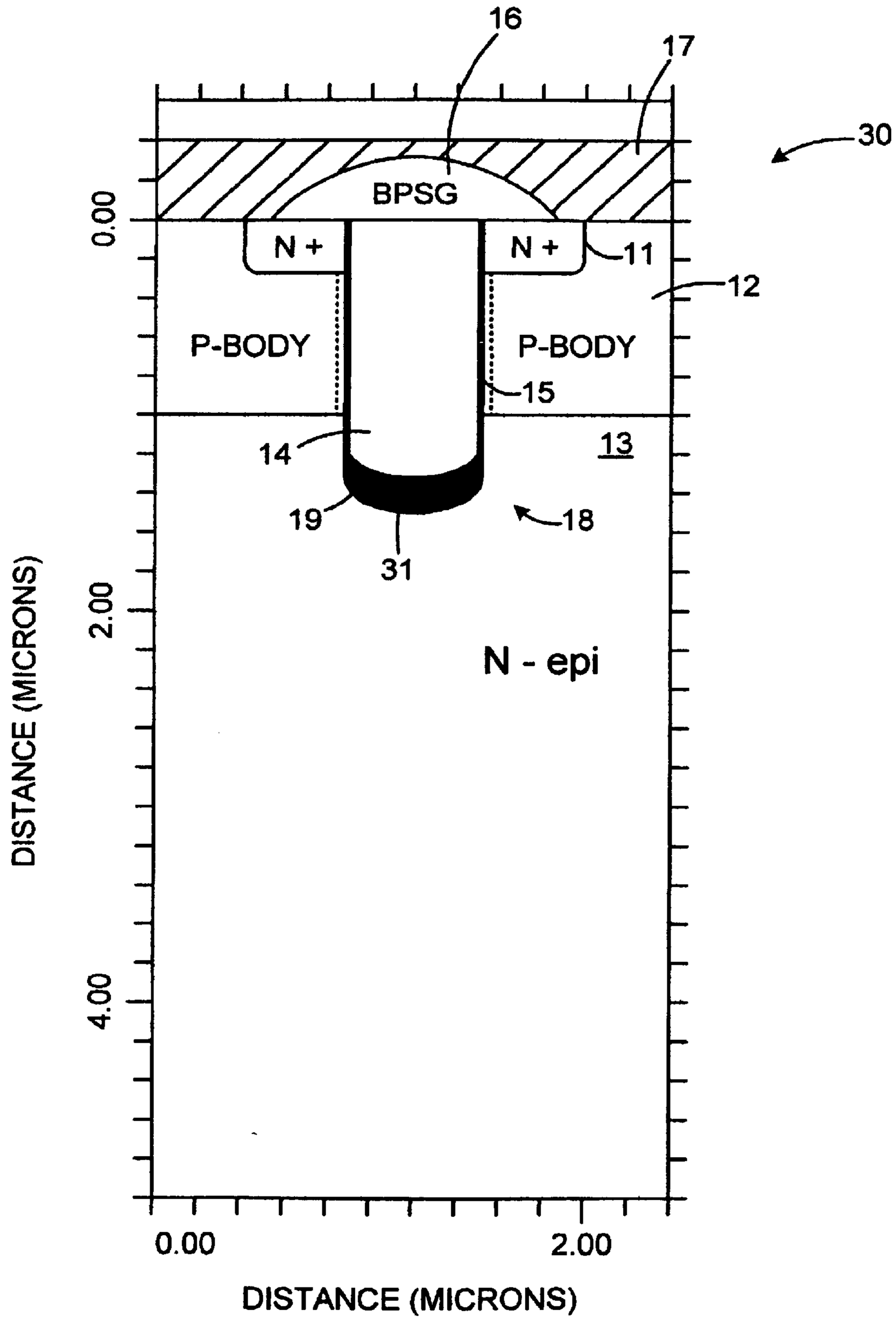

16
17
30
BPSG
0.00
N +
N +
11
12
P-BODY
P-BODY
15
14
13
19
18
31
N - epi
2.00
4.00
DISTANCE (MICRONS)
0.00
2.00
DISTANCE (MICRONS)

FIG. 3

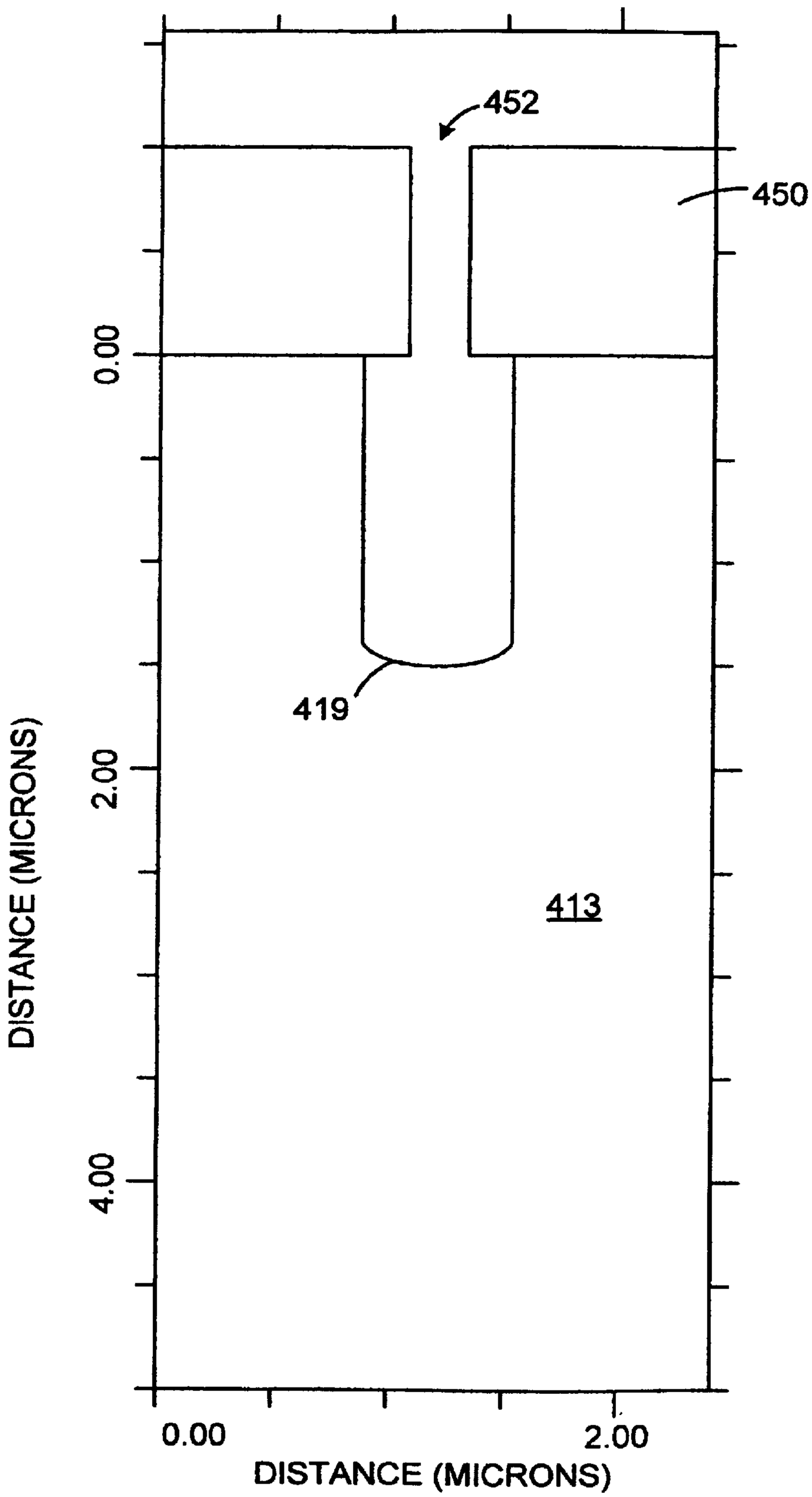

452
450
419
413
0.00
2.00
4.00
DISTANCE (MICRONS)
0.00
2.00
DISTANCE (MICRONS)

FIG. 4A

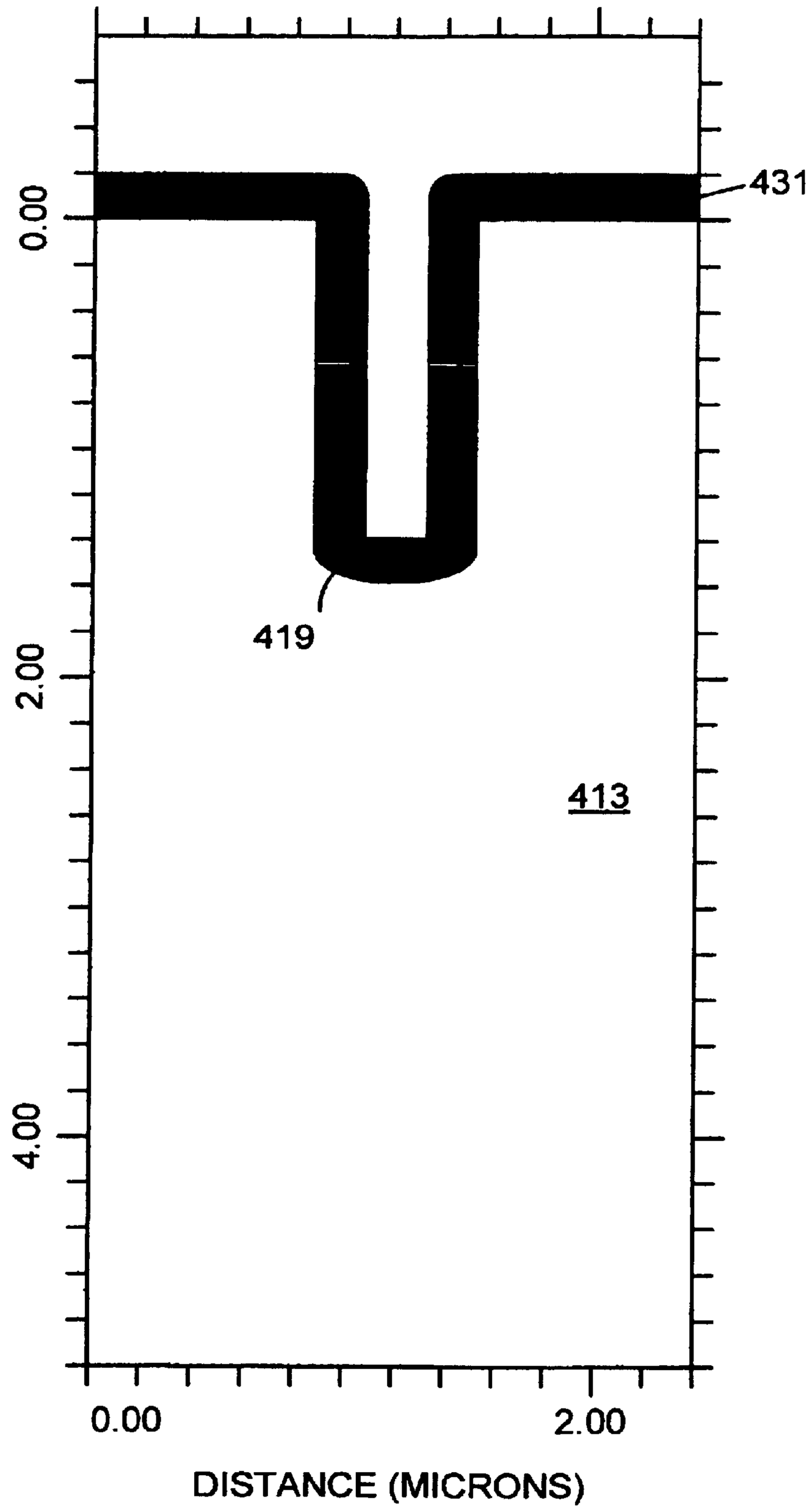

0.00
2.00
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431
419
413
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DISTANCE (MICRONS)

FIG. 4B

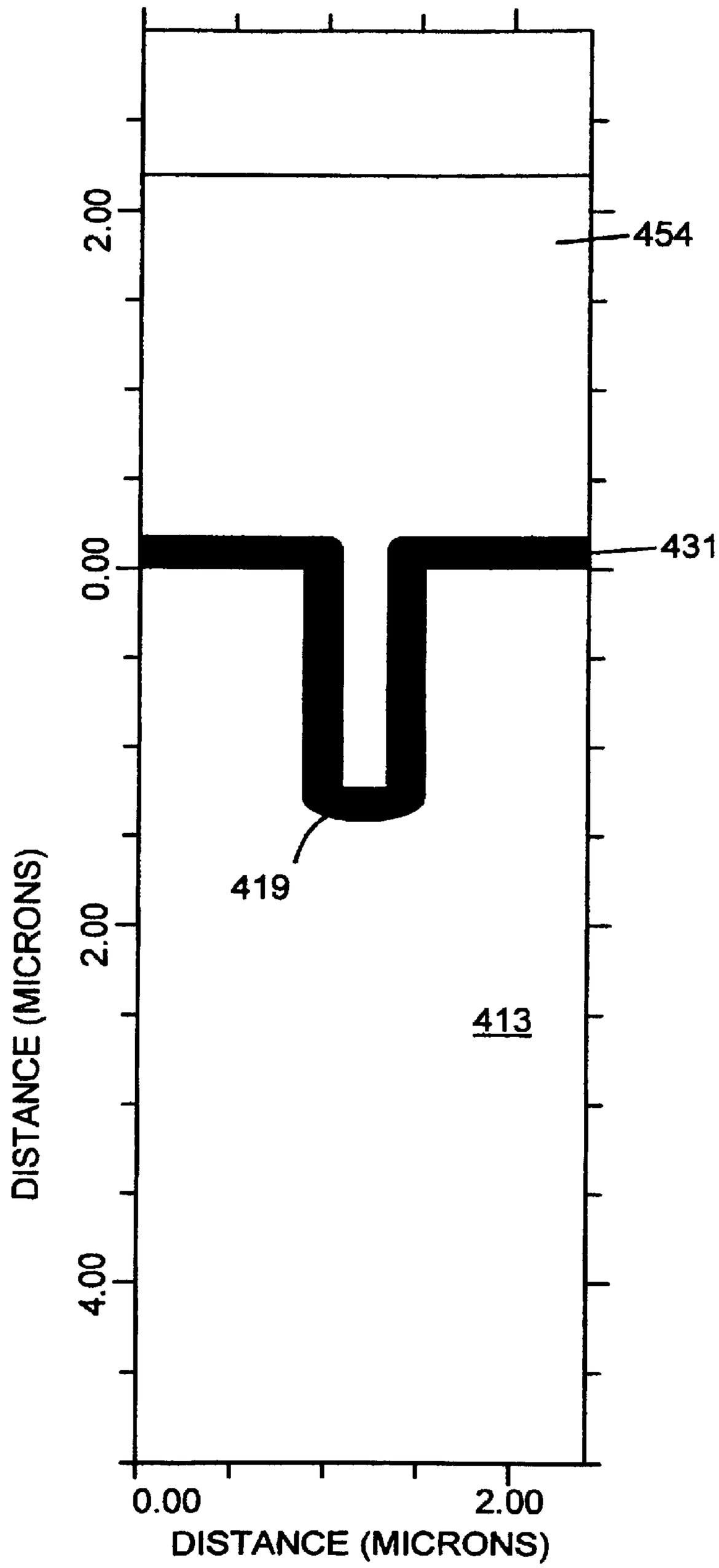

2.00
454
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431
419
2.00
413
DISTANCE (MICRONS)
4.00
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2.00
DISTANCE (MICRONS)

FIG. 4C

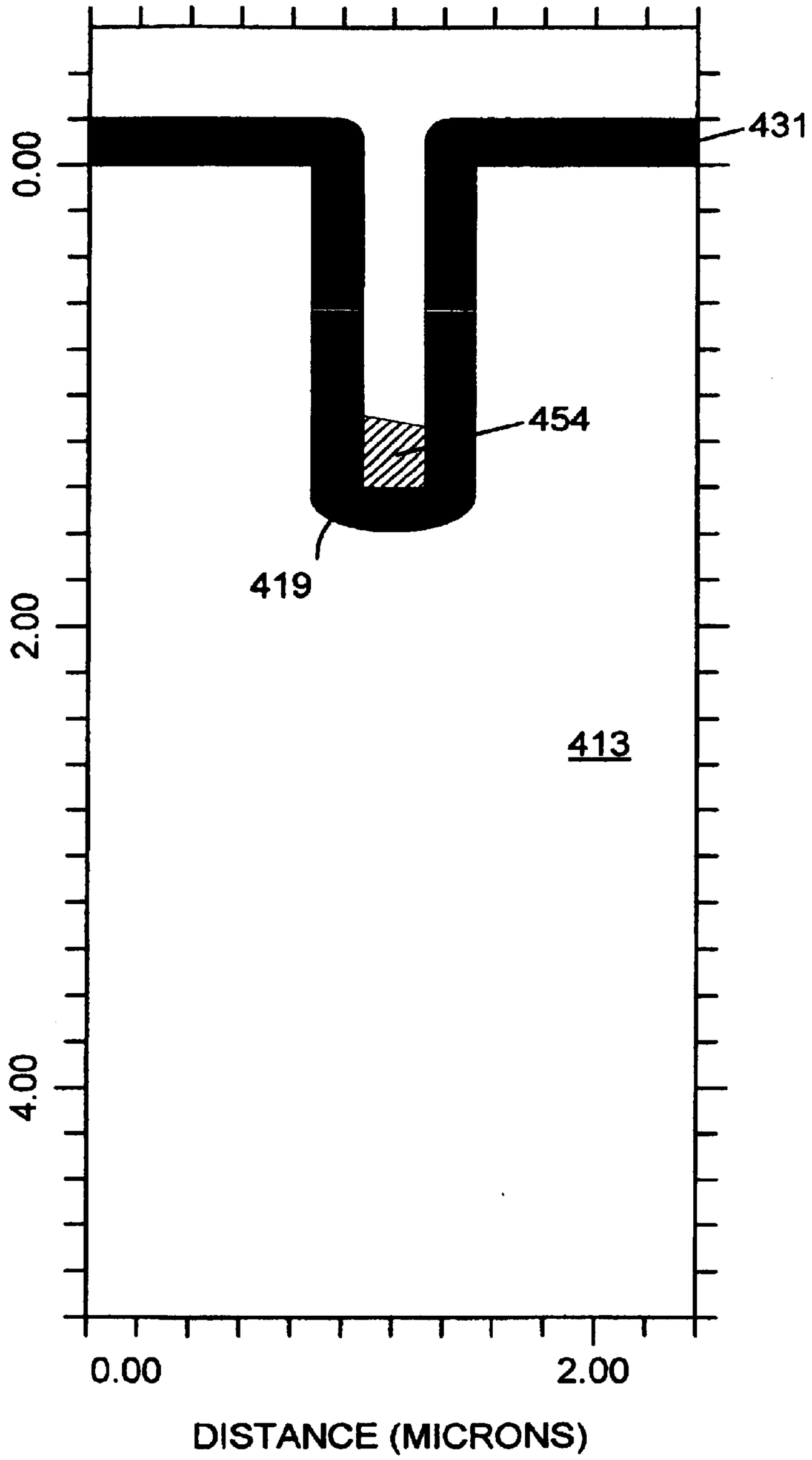

0.00
2.00
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DISTANCE (MICRONS)
431
454
419
413
0.00
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DISTANCE (MICRONS)

FIG. 4D

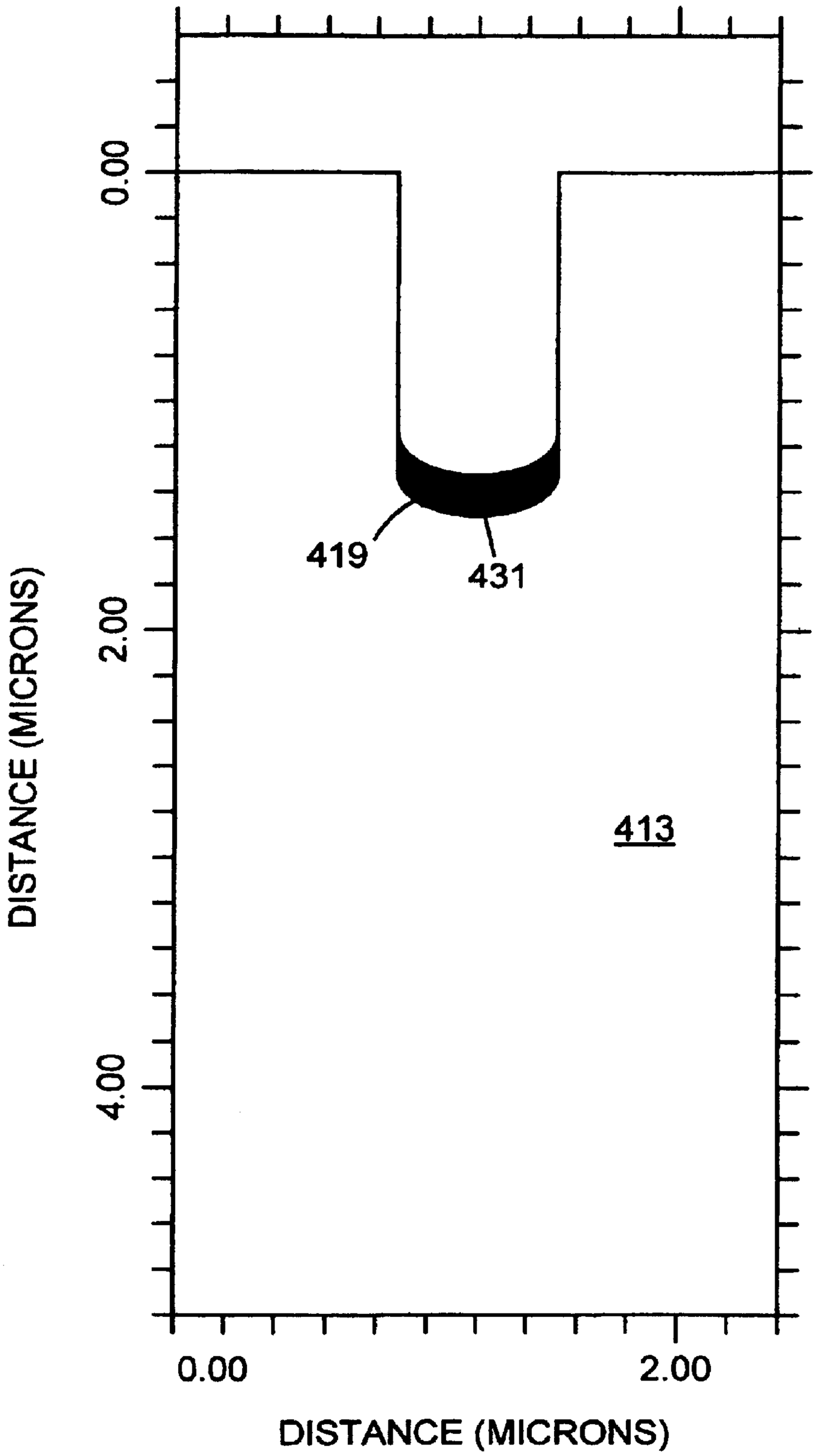

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DISTANCE (MICRONS)
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431
413
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2.00
DISTANCE (MICRONS)

FIG. 4E

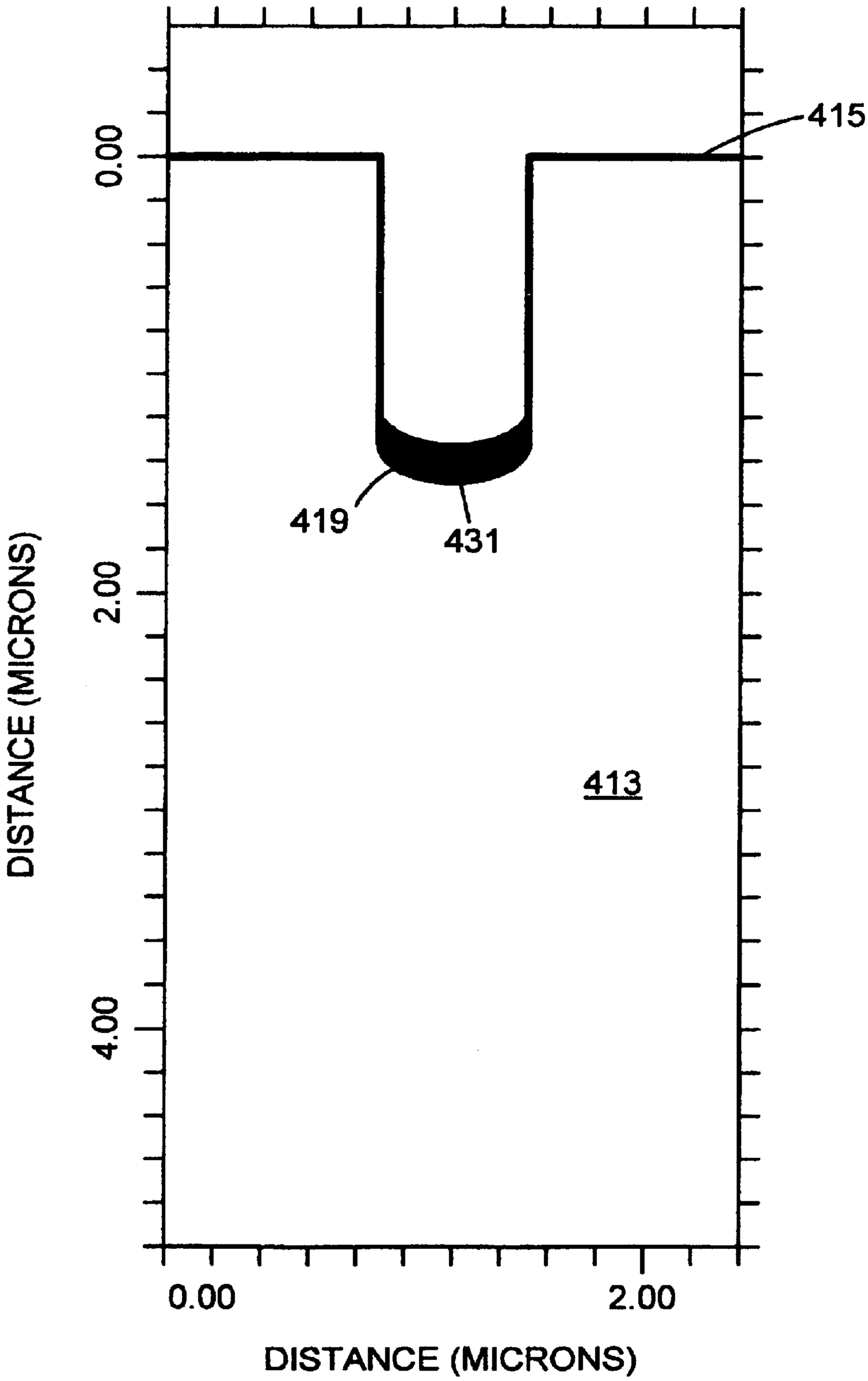

0.00
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4.00
DISTANCE (MICRONS)
415
419
431
413
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2.00
DISTANCE (MICRONS)

FIG. 4F

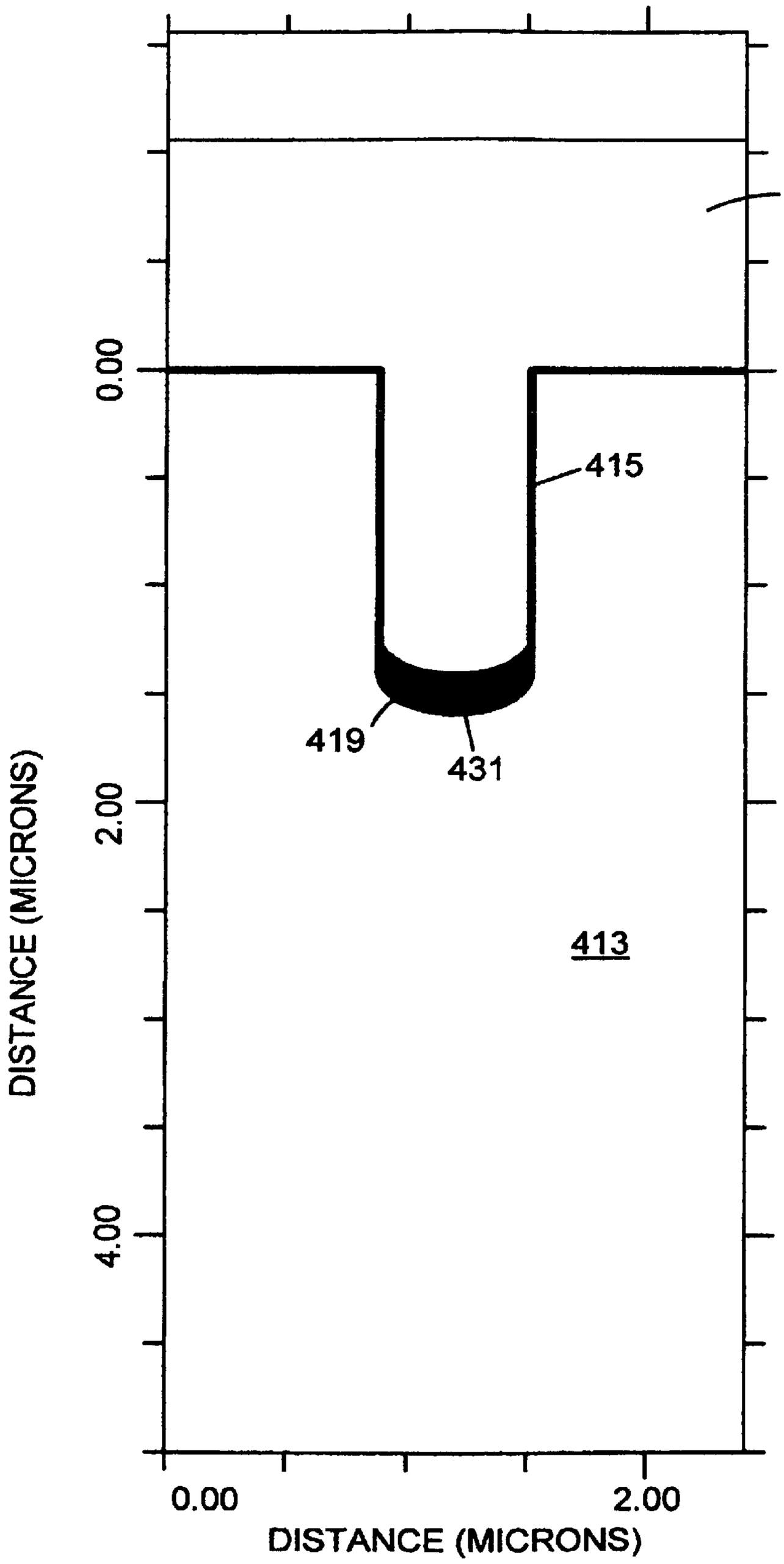

456
415
419
431
413
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2.00
4.00
DISTANCE (MICRONS)
0.00
2.00
DISTANCE (MICRONS)

FIG. 4G

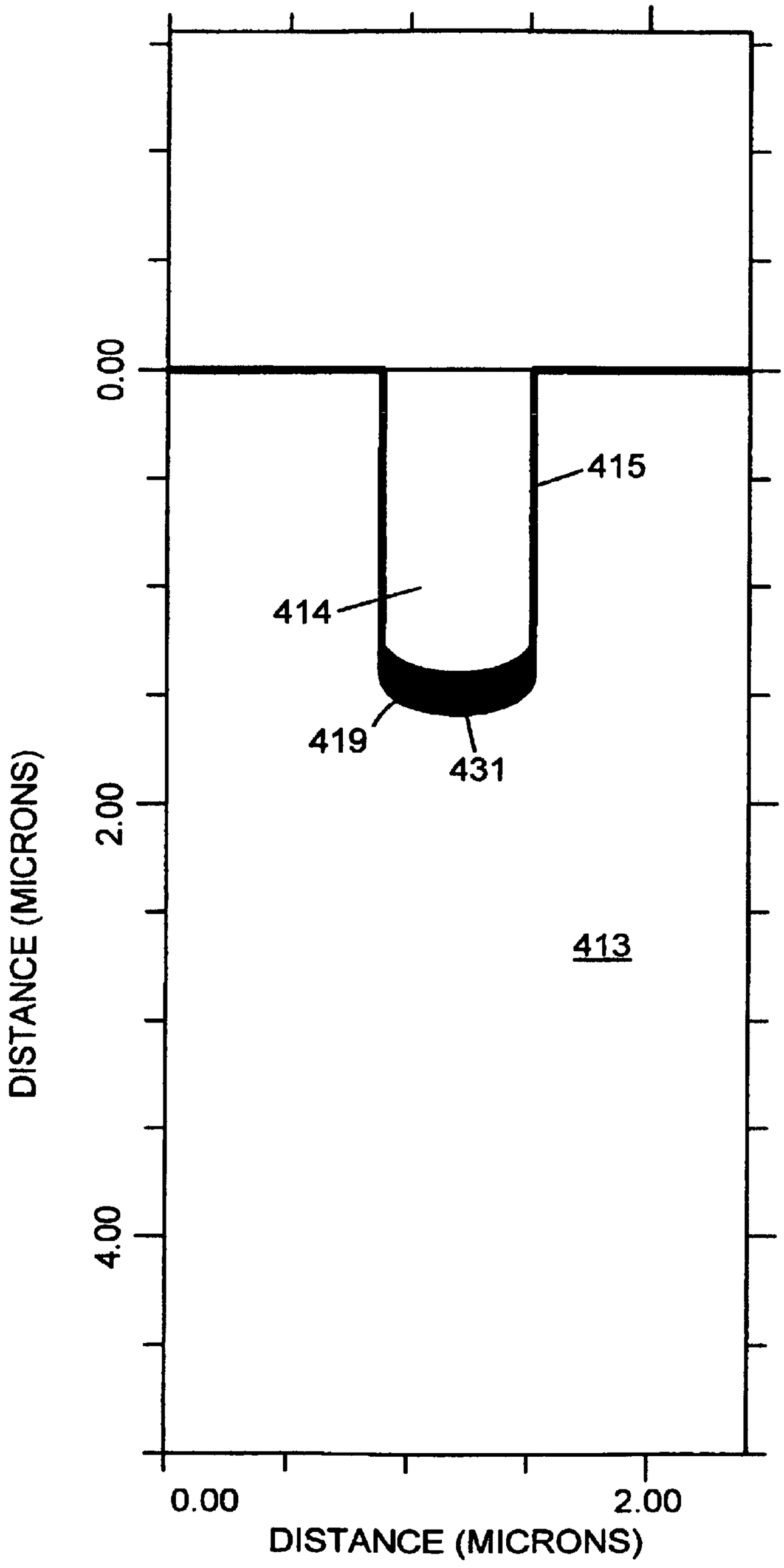

0.00
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4.00
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414
419
431
413
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2.00
DISTANCE (MICRONS)

FIG. 4H

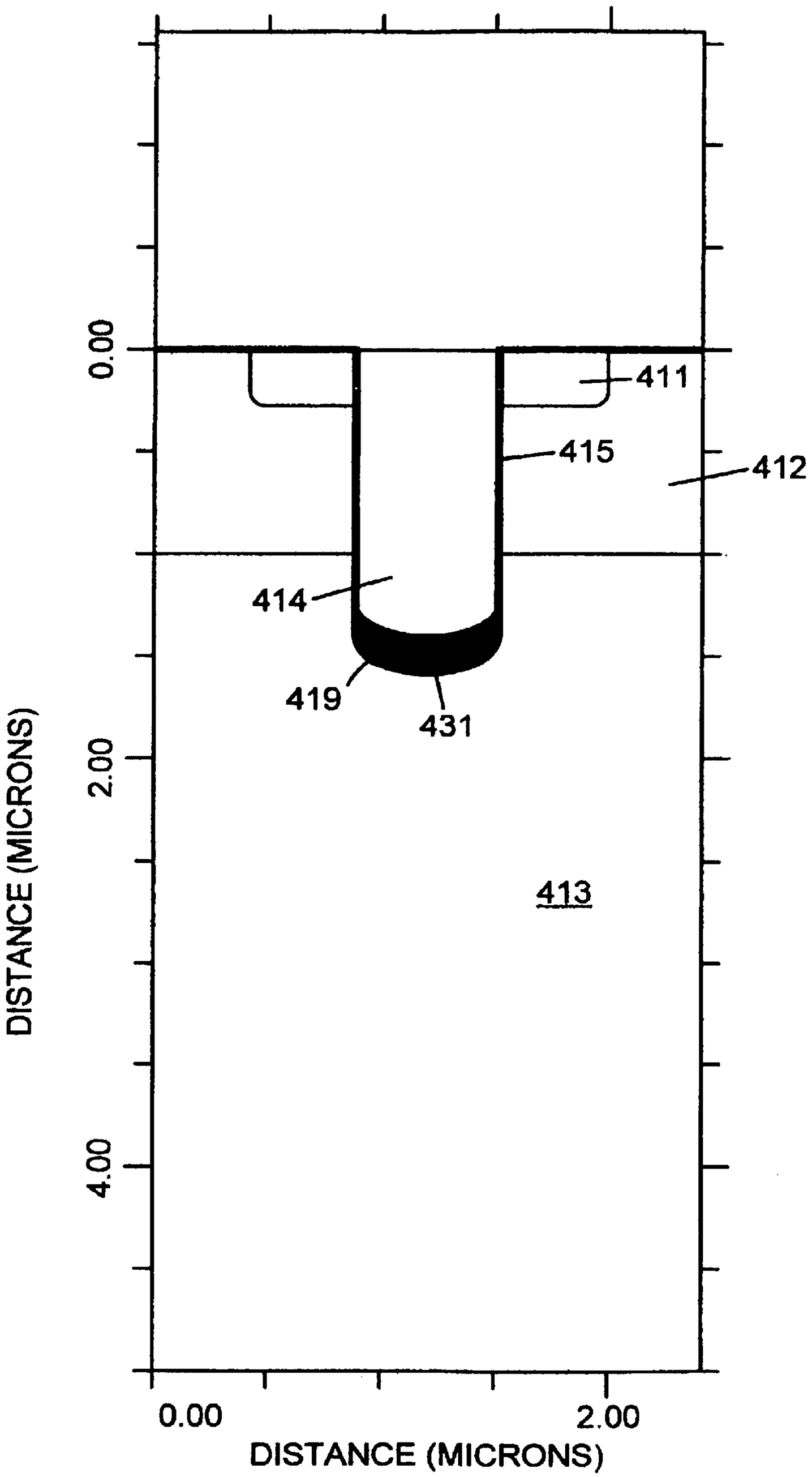

0.00
2.00
4.00
DISTANCE (MICRONS)
411
415
412
414
419
431
413
0.00
2.00
DISTANCE (MICRONS)

FIG. 4I

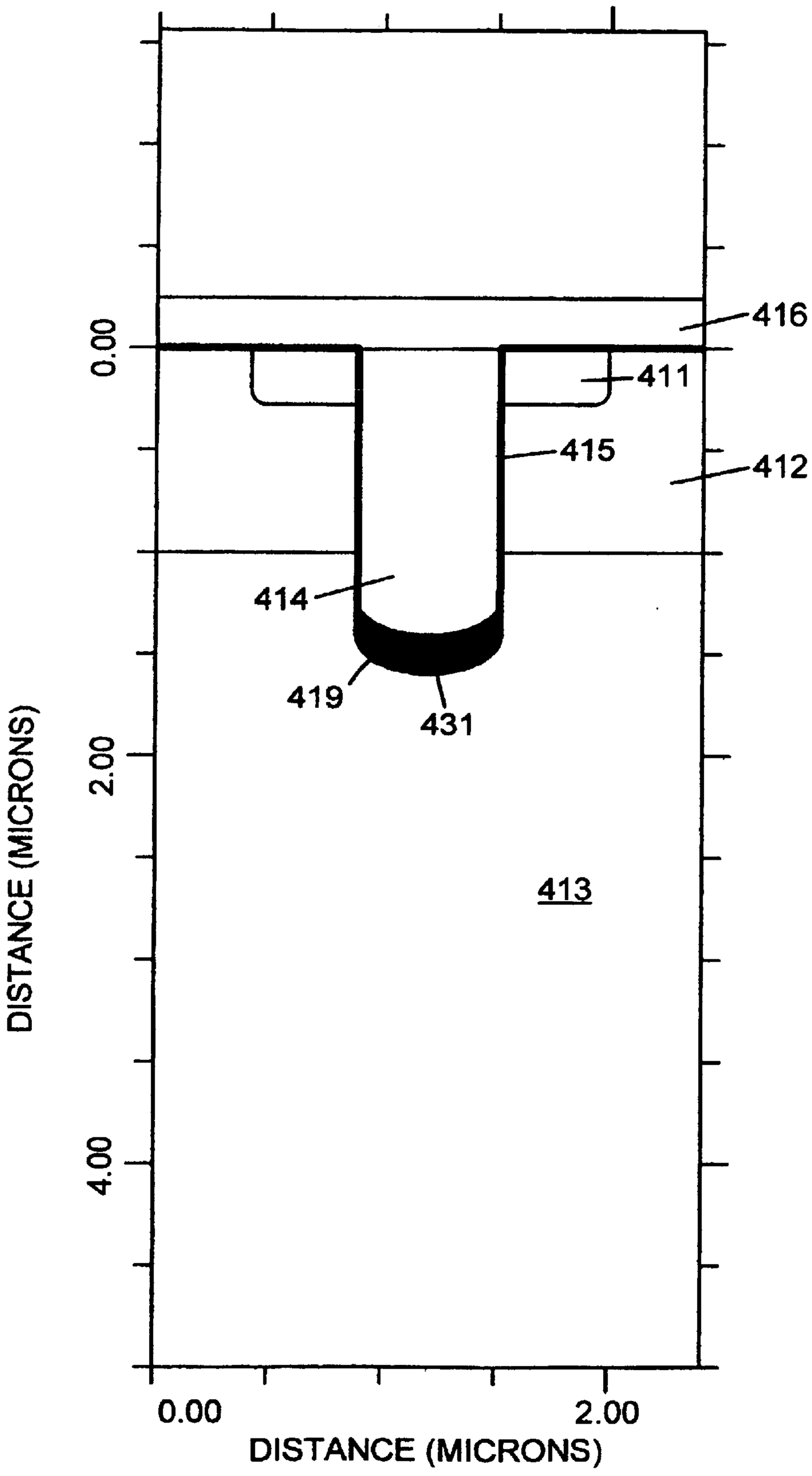

0.00
2.00
4.00
DISTANCE (MICRONS)
0.00
2.00
DISTANCE (MICRONS)
416
411
415
412
414
419
431
413

FIG. 4J

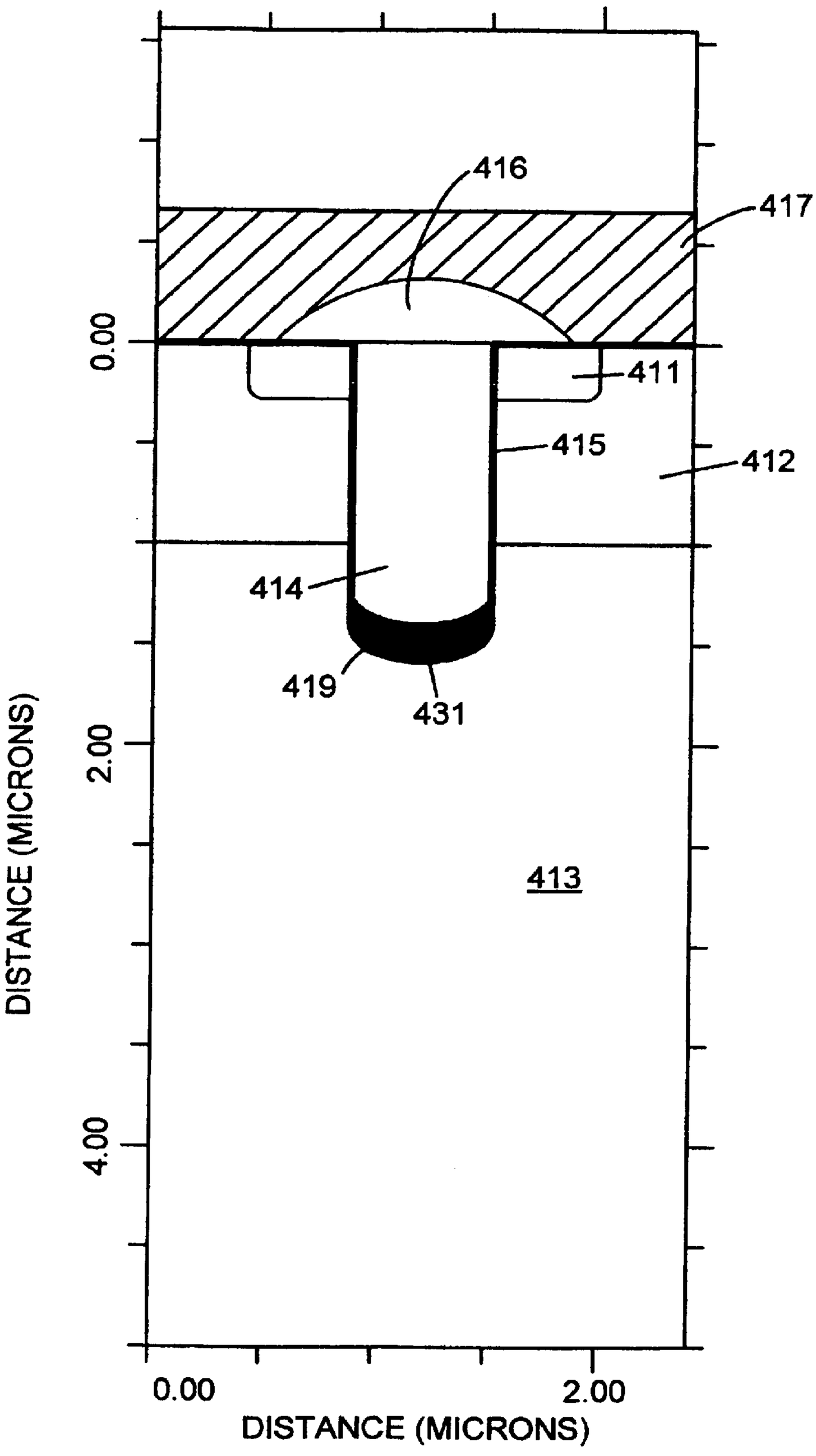

416
417
411
415
412
414
419
431
413
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2.00
4.00
DISTANCE (MICRONS)
0.00
2.00
DISTANCE (MICRONS)

FIG. 4K

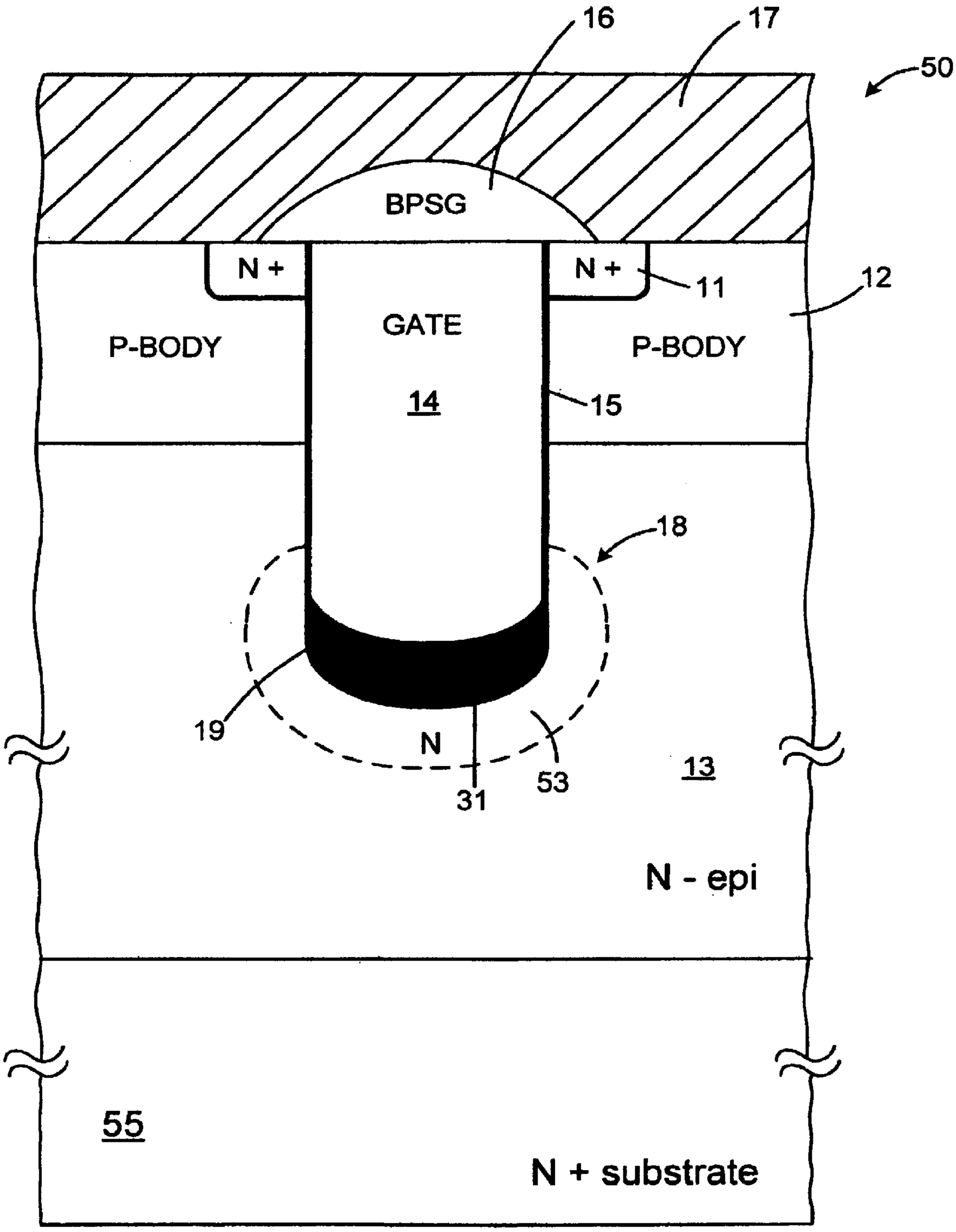

16
17
50
BPSG
N +
N +
11
12
P-BODY
GATE
14
P-BODY
15
18
19
N
31
53
13
N - epi
55
N + substrate

FIG. 5

TRENCH MIS DEVICE WITH REDUCED GATE-TO-DRAIN CAPACITANCE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to application Ser. No. 09/591,179, filed Jun. 8, 2000, which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

This invention relates to trench metal-insulator-semiconductor (MIS) devices and in particular to trench MOSFETs that are suitable for high frequency operation.

BACKGROUND

Some metal-insulator-semiconductor (MIS) devices include a gate located in a trench that extends downward from the surface of a semiconductor substrate (e.g., silicon). The current flow in such devices is primarily vertical and, as a result, the cells can be more densely packed. All else being equal, this increases the current carrying capability and reduces the on-resistance of the device. Devices included in the general category of MIS devices include metal-oxide-semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), and MOS-gated thyristors.

Trench MOSFETs, for example, can be fabricated with a high transconductance ($g_{m,max}$) and low specific on resistance (R_{on}), which are important for optimal linear signal amplification and switching. One of the most important issues for high frequency operation, however, is reduction of the MOSFET internal capacitances. The internal capacitances include the gate-to-drain capacitance (C_{gd}), which is also called the feedback capacitance (C_{rss}), the input capacitance (C_{iss}), and the output capacitance (C_{oss}).

FIG. **1** is a cross-sectional view of a conventional n-type trench MOSFET **10**. In MOSFET **10**, an n-type epitaxial ("N-epi") layer **13**, which is usually grown on an N^+ substrate (not shown), is the drain. N-epi layer **13** may be a lightly doped layer, that is, an N^- layer. A p-type body region **12** separates N-epi layer **13** from N^+ source regions **11**. Current flows vertically through a channel (denoted by the dashed lines) along the sidewall of a trench **19**. The sidewall and bottom of trench **19** are lined with a thin gate insulator **15** (e.g., silicon dioxide). Trench **19** is filled with a conductive material, such as doped polysilicon, which forms a gate **14**. Trench **19**, including gate **14** therein, is covered with an insulative layer **16**, which may be borophosphosilicate glass (BPSG). Electrical contact to source regions **11** and body region **12** is made with a conductor **17**, which is typically a metal or metal alloy. Gate **14** is contacted in the third dimension, outside of the plane of FIG. **1**.

A significant disadvantage of MOSFET **10** is a large overlap region **18** formed between gate **14** and N-epi layer **13**, which subjects a portion of thin gate insulator **15** to the drain operating voltage. The large overlap limits the drain voltage rating of MOSFET **10**, presents long term reliability issues for thin gate insulator **15**, and greatly increases the gate-to-drain capacitance, C_{gd}, of MOSFET **10**. In a trench structure, C_{gd} is larger than in conventional lateral devices, limiting the switching speed of MOSFET **10** and thus its use in high frequency applications.

One possible method to address this disadvantage is described in the above-referenced application Ser. No. 09/591,179 and is illustrated in FIG. **2**. FIG. **2** is a cross-sectional view of a trench MOSFET **20** with an undoped polysilicon plug **22** near the bottom of trench **19**. MOSFET **20** is similar to MOSFET **10** of FIG. **1**, except for polysilicon plug **22**, which is isolated from the bottom of trench **19** by oxide layer **21** and from gate **14** by oxide layer **23**. The sandwich of oxide layer **21**, polysilicon plug **22**, and oxide layer **23** serves to increase the distance between gate **14** and N-epi layer **13**, thereby decreasing C_{gd}.

In some situations, however, it may be preferable to have a material even more insulative than undoped polysilicon in the bottom of trench **19** to minimize C_{gd} for high frequency applications. Accordingly, a trench MOSFET with decreased gate-to-drain capacitance, C_{gd}, and better high frequency performance is desirable.

SUMMARY

In accordance with the present invention, a metal-insulator-semiconductor (MIS) device includes a semiconductor substrate including a trench extending into the substrate from a surface of the substrate. A source region of a first conductivity type is adjacent to a sidewall of the trench and to the surface of the substrate. A body region of a second conductivity type opposite to the first conductivity type is adjacent to the source region and to the sidewall. A drain region of the first conductivity type is adjacent to the body region and to the sidewall. The trench is lined with a first insulative layer along a portion of the sidewall that abuts the body region. The trench is also lined with a second insulative layer along a bottom portion of the trench. The second insulative layer is coupled to the first insulative layer, and the second insulative layer is thicker than the first insulative layer. The stress in the substrate along the bottom portion of the trench does not change appreciably.

In an exemplary embodiment of a fabrication process for such an MIS device, a trench including a sidewall and a bottom is formed in a substrate. A thick insulative layer is deposited on the bottom of the trench. A thin insulative layer is formed on the sidewall, and is coupled to the thick insulative layer. A gate is formed above the portion of the thick insulative layer and adjacent to the thin insulative layer in the trench.

The thick insulative layer separates the trench gate from the drain conductive region at the bottom of the trench resulting in a reduced gate-to-drain capacitance. This makes MIS devices in accordance with the present invention, such as trench MOSFETs, suitable for high frequency applications.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention will be better understood by reference to the following description and drawings. In the drawings, like or similar features are typically labeled with the same reference numbers.

FIG. **1** is a cross-sectional view of a conventional trench MOSFET.

FIG. **2** is a cross-sectional view of a trench MOSFET with a polysilicon plug at the bottom of the trench.

FIG. **3** is a cross-sectional view of one embodiment of a trench MOSFET in accordance with the present invention.

FIGS. **4A–4K** are cross-sectional views illustrating one embodiment of a process for fabricating a trench MOSFET in accordance with the present invention.

FIG. **5** is a cross-sectional view of an alternative embodiment of a trench MOSFET in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **3** is a cross-sectional view of one embodiment of a trench MOSFET **30** in accordance with the present invention. MOSFET **30** has some similarities to MOSFET **10** of

FIG. **1**. The elements of MOSFET **30** outside of trench **19** can be the same as those of MOSFET **10** of FIG. **1**. In MOSFET **30**, however, only the sidewall of trench **19** is lined with thin gate insulator **15** (e.g., silicon dioxide). Unlike MOSFET **10** of FIG. **1**, a thick insulative layer **31** (e.g., silicon dioxide) lines the bottom of trench **19** of MOSFET **30** of FIG. **3**. Thick insulative layer **31** separates gate **14** from N-epi layer **13** (which may be an N^- layer). This circumvents the problems that occur when only thin gate insulator **15** separates gate **14** from N-epi layer **13** (the drain) as in FIG. **1**. Thick insulative layer **31** also provides a more effective insulator than is achievable with polysilicon plug **22** as shown in FIG. **2**. Thus, thick insulative layer **31** minimizes the gate-to-drain capacitance, C_{gd}, and yields a trench MOSFET **30** useful for high frequency applications.

FIGS. **4A–4K** are cross-sectional views illustrating one embodiment of a process for fabricating a trench MOSFET, such as MOSFET **30** of FIG. **3**, in accordance with the present invention. As shown in FIG. **4A**, the process begins with a lightly-doped N-epi layer **413** (typically about 8 μm thick) grown on a heavily doped N^+ substrate (not shown). A trench mask **450**, which may be photoresist or an oxide, is deposited on N-epi layer **413** and patterned to form an opening **452** where a trench **419** is to be located. Trench **419** is etched through opening **452**, typically using a dry plasma etch, for example, a reactive ion etch (RIE). Trench **419** may be about 0.5–1.2 μm wide and about 1–2 μm deep.

Mask **450** is removed, and a thick insulative layer **431** (e.g., about 0.1–0.3 μm) is deposited on N-epi layer **413**, as shown in FIG. **4B**. The deposition process is chosen, according to conventional deposition techniques such as chemical vapor deposition (CVD), to yield conformal deposition of insulative layer **431** on the sidewall and bottom of trench **419**, as well as on the top surface of N-epi layer **413**. Thick insulative layer **431** may be, for example, a low temperature oxide (LTO), a phosphosilicate glass (PSG), a BPSG, or another insulative material. In some embodiments, a thin insulative layer (e.g., 100–200 Å of silicon dioxide) could be thermally grown, for example, using a well known dry oxidation process at 950° C. for 10 minutes, prior to deposition of thick insulative layer **431**.

As shown in FIG. **4C**, a barrier layer **454** is then deposited by CVD. This deposition can be non-conformal, filling trench **419** and overflowing past the topmost surface of thick insulative layer **431**. Barrier layer **454** may be, for example, silicon nitride (Si_3N_4), and may be 2–4 μm thick. Barrier layer **454** is etched back, typically by performing a dry etch followed by a wet etch, using etchants that have high selectivity for barrier layer **454** over thick insulative layer **431**. Barrier layer **454** is etched back into trench **419** until only about 0.1–0.2 μm remains in trench **419**, as shown in FIG. **4D**.

Thick insulative layer **431** is then etched, typically by a wet etch technique, using an etchant that has high selectivity for insulative layer **431** over barrier layer **454** and over N-epi layer **413**. Insulative layer **431** is etched from the top of N-epi layer **413** and from the sidewall of trench **419** until insulative layer **431** remains only in the bottom of trench **431**. The remainder of barrier layer **454** is removed, leaving the structure shown in FIG. **4E**.

As shown in FIG. **4F**, a thin gate insulator **415** (e.g., about 100–1000 Å thick) is then formed on the top surface of N-epi layer **413** and on the sidewall of trench **419**. Thin gate insulator **415** may be, for example, a silicon dioxide layer that is thermally grown using a dry oxidation technique at 1050° C. for 20 minutes. In some embodiments, a sacrificial gate oxide (not shown) can be thermally grown and removed by a wet etch to clean the sidewall of trench **419** prior to growing thin gate insulator **415**. The wet etch of such a sacrificial gate oxide is kept short to minimize etching of thick insulative layer **431**.

As shown in FIG. **4G**, a conductive material **456** is deposited by CVD, possibly by low pressure CVD (LPCVD), to fill trench **419** and overflow past the topmost surface of thin gate insulator **415**. Conductive material **456** may be, for example, an in-situ doped polysilicon, or an undoped polysilicon layer that is subsequently implanted and annealed, or an alternative conductive material. Conductive material **456** is etched, typically using a reactive ion etch, until the top surface of material **456** is approximately level with the top of N-epi layer **413**, thereby forming gate **414**, as shown in FIG. **4H**. In an n-type MOSFET, gate **414** may be, for example, a polysilicon layer with a doping concentration of 10^{20} cm^{-3}. In some embodiments, conductive material **456** may be etched past the top of trench **419**, thereby recessing gate **414** to minimize the gate-to-source overlap capacitance.

Using known implantation and diffusion processes, p-type body regions **412** and N^+ source regions **411** are formed in N-epi layer **413** as shown in FIG. **4I**. The PN junctions between p-type body regions **412** and the remainder of N-epi layer **413** are located at a depth above the interface between thick insulative layer **431** and thin gate insulator **415**.

As shown in FIG. **4J**, an insulative layer **416**, which may be borophosphosilicate glass (BPSG), is deposited by CVD on the surfaces of N-epi layer **413** and gate **414**. Insulative layer **416** is etched, typically using a dry etch, to expose portions of p-type body regions **412** and N^+ source regions **411**, as shown in FIG. **4K**. Electrical contact to body regions **412** and source regions **411** is made with a conductor **417**, which is typically a deposited (e.g., by physical vapor deposition, plating, sputtering, or evaporation) metal or metal alloy. Electrical contact to gate **414** is made in the third dimension, outside of the plane of FIG. **4K**. Electrical contact to the drain (not shown) is made to the opposite surface of the N^+ substrate (not shown) on which N-epi layer **413** is grown.

This method thus allows incorporation of thick insulative layer **431** at the bottom of trench **419** to minimize C_{gd} with minimal undesirable effects or manufacturing concerns, which may be caused by thermally growing thick insulative layer **431**. For example, stress effects from growing a thick oxide in the concave bottom of trench **419** are avoided by depositing the oxide rather than thermally growing it. Thinning of the insulative layers at the juncture of thick insulative layer **431** and thin gate insulator **415**, possibly caused by formation of a "bird's beak" during a thermal growth of thick insulative layer **431**, are avoided by depositing thick insulative layer **431**. In addition, shifts in the etched sidewall profile of trench **419** are also avoided by depositing thick insulative layer **431**. Growing thick insulative layer **431** could cause such shifts, resulting in a "bulb" effect at the bottom of trench **419** that is not compensated by subsequent growth of thin gate insulator **415** on the sidewall of trench **419**.

FIG. **5** is a cross-sectional view of an alternative embodiment of a trench MOSFET **50** in accordance with the present invention. MOSFET **50** has many similarities to MOSFET **30** of FIG. **3**. In particular, only the sidewall of trench **19** is lined with thin gate insulator **15**, while thick insulative layer **31** lines the bottom of trench **19**. In MOSFET **30** of FIG. **3**, thick insulative layer **31** may increase the on-resistance (R_{on}) of MOSFET **30** due to an increase in the spreading resistance in the accumulation layer at the bottom of trench **19**. MOSFET **50** of FIG. **5**, however, includes a high doping region **53** at the bottom of trench **19** to help spread current more effectively. High doping region **53** is formed in N-epi layer **13**, which overlies an N^+ substrate **55**. High doping region **53** may be created by implanting an n-type dopant, such as arsenic or phosphorous, before mask **450** is removed after the trench etch shown in FIG. **4A**. Thus, thick insula-

tive layer **31** minimizes gate-to-drain capacitance, C_{gd}, and high doped region **53** minimizes on-resistance, R_{on}, yielding a trench MOSFET **50** well-suited for high frequency applications.

The foregoing embodiments are intended to be illustrative and not limiting of the broad principles of this invention. Many additional embodiments will be apparent to persons skilled in the art. For example, the structures and methods of this invention can be used with any type of metal-insulator-semiconductor (MIS) device in which it is desirable to form an insulating layer between a trench gate and a region outside the trench. Also, various insulative or conductive materials can be used where appropriate, and the invention is also applicable to p-type MOSFETs. The invention is limited only by the following claims.

We claim:

1. A metal-insulator-semiconductor device comprising:

a first drain region;

a body region disposed on a first surface of said first drain region;

a gate region extending through said body region and partially into said first drain region;

a source region disposed between a first portion of said body region and a first portion of said gate region;

a first insulative layer disposed between said source region and said first portion of said gate region and between said body region and a second portion of said gate region, wherein a thickness of said first insulative layer is in the range of approximately 100 to 1000 Å; and

a second insulative layer disposed at least partially between a first portion of said first drain region and a third portion of said gate region and adjacent to said first insulative layer, wherein a thickness of said second insulative layer is in the range of approximate 0.1 to 0.3 μm, wherein said second insulative layer is not formed by oxidizing said first drain region and wherein said second insulative layer does not introduce substantial stress in said first drain region.

2. The metal-insulator-semiconductor device according to claim **1**, wherein said gate region comprises polysilicon.

3. The metal-insulator-semiconductor device according to claim **1**, further comprising a highly doped region formed in said first drain region adjacent said third portion of said gate region.

4. The metal-insulator-semiconductor device according to claim **1**, wherein said first insulative layer comprises an oxide.

5. The metal-insulator-semiconductor device according to claim **1**, wherein said second insulative layer is selected from the group consisting of phosphosilicate glass and borophosphosilicate glass.

6. A metal-insulator-semiconductor device comprising:

a first drain region;

a body region disposed on a first surface of said first drain region;

a gate region extending through said body region and partially into said first drain region;

a source region disposed between a first portion of said body region and a first portion of said gate region;

an oxide layer disposed between said source region and said first portion of said gate region, between a second portion of said body region and a second portion of said gate region and between a first portion of said first drain region and a third portion of said gate region, wherein a thickness of said oxide layer is in the range of approximate 100 to 1000 Å; and

an insulative layer, selected from a group of material consisting of phosphosilicate glass and borophosphosilicate glass, disposed between a second portion of said first drain region and a fourth portion of said gate region and coupled to said oxide layer, wherein a thickness of said insulative layer is in the ranger of approximate 0.1 to 0.3 μm and wherein said insulative layer does not introduce substantial stress in said second portion of said first drain region.

7. The metal-insulator-semiconductor device according to claim **6**, wherein said first drain region comprises a semiconductor of a first conductive type.

8. The metal-insulator-semiconductor device according to claim **6**, wherein said body region comprises a semiconductor of a second conductive type.

9. The metal-insulator-semiconductor device according to claim **6**, wherein said source region comprises a semiconductor of a first conductive type.

10. The metal-insulator-semiconductor device according to claim **6**, further comprising a second drain region disposed on a second surface of said first drain region, wherein said second surface is opposite said first surface.

11. The metal-insulator-semiconductor device according to claim **10**, wherein said second drain region comprises a semiconductor of a first conductive type semiconductor.

12. A metal-insulator-semiconductor device comprising:

a first drain region;

a body region disposed above said first drain region;

a gate region extending through said body region and partially into said first drain region;

a source region disposed between a first portion of said body region and a first portion of said gate region;

a silicon dioxide layer disposed between said source region and said first portion of said gate region, between a second portion of said body region and a second portion of said gate region and between a first portion of said first drain region and a third portion of said gate region, wherein a thickness of said silicon dioxide layer is in the rage of approximate 100 to 1000 Å; and

an insulative layer, selected from a group of material consisting of phosphosilicate glass and borophosphosilicate glass, disposed between a second portion of said first drain region and a fourth portion of said gate region and coupled to said silicon dioxide layer, wherein a thickness of said insulative layer is in the range of approximately 0.1 to 0.3 μm and wherein said insulative layer does not introduce substantial stress in said first drain region.

13. The metal-insulator-semiconductor device according to claim **12**, wherein said first drain region comprises a lightly n-doped semiconductor.

14. The metal-insulator-semiconductor device according to claim **13**, wherein said body region comprises a p-doped semiconductor.

15. The metal-insulator-semiconductor device according to claim **14**, wherein said source region comprises a heavily n-doped semiconductor.

16. The metal-insulator-semiconductor device according to claim **15**, further comprising a second drain region disposed below said first drain region.

17. The metal-insulator-semiconductor device according to claim **16**, wherein said second drain region comprises a heavily n-doped semiconductor.

18. The metal-insulator-semiconductor device according to claim **17**, wherein said gate region comprises polysilicon.

19. The metal-insulator-semiconductor device according to claim **18**, further comprising an n-doped semiconductor region disposed in said first drain region adjacent said fourth portion of said gate region.

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