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(54) **SEMICONDUCTOR RADIO FREQUENCY SWITCH WITH BODY CONTACT**

(75) Inventors: **Michael Carroll**, Jamestown, NC (US);
Daniel Charles Kerr, Oak Ridge, NC (US); **Christian Rye Iversen**, Vestbjerg (DK); **Philip Mason**, Greensboro, NC (US); **Julio Costa**, Oak Ridge, NC (US);
Edward T. Spears, Oak Ridge, NC (US)

(73) Assignee: **RF Micro Devices, Inc.**, Greensboro, NC (US)

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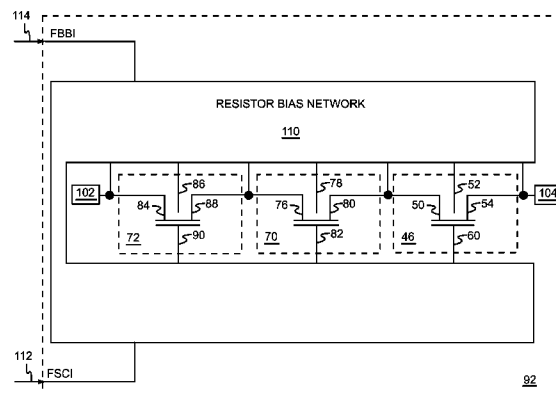
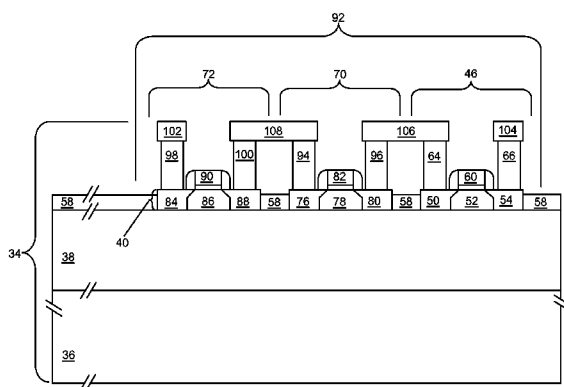
Primary Examiner — Eugene Lee

(74) *Attorney, Agent, or Firm* — Withrow & Terranova, P.L.L.C.

(57) **ABSTRACT**

The present disclosure relates to a radio frequency (RF) switch that includes multiple body-contacted field effect transistor (FET) elements coupled in series. The FET elements may be formed using a thin-film semiconductor device layer, which is part of a thin-film semiconductor die. Conduction paths between the FET elements through the thin-film semiconductor device layer and through a substrate of the thin-film semiconductor die may be substantially eliminated by using insulating materials. Elimination of the conduction paths allows an RF signal across the RF switch to be divided across the series coupled FET elements, such that each FET element is subjected to only a portion of the RF signal. Further, each FET element is body-contacted and may receive reverse body biasing when the RF switch is in an OFF state, thereby reducing an OFF state drain-to-source capacitance of each FET element.

25 Claims, 20 Drawing Sheets



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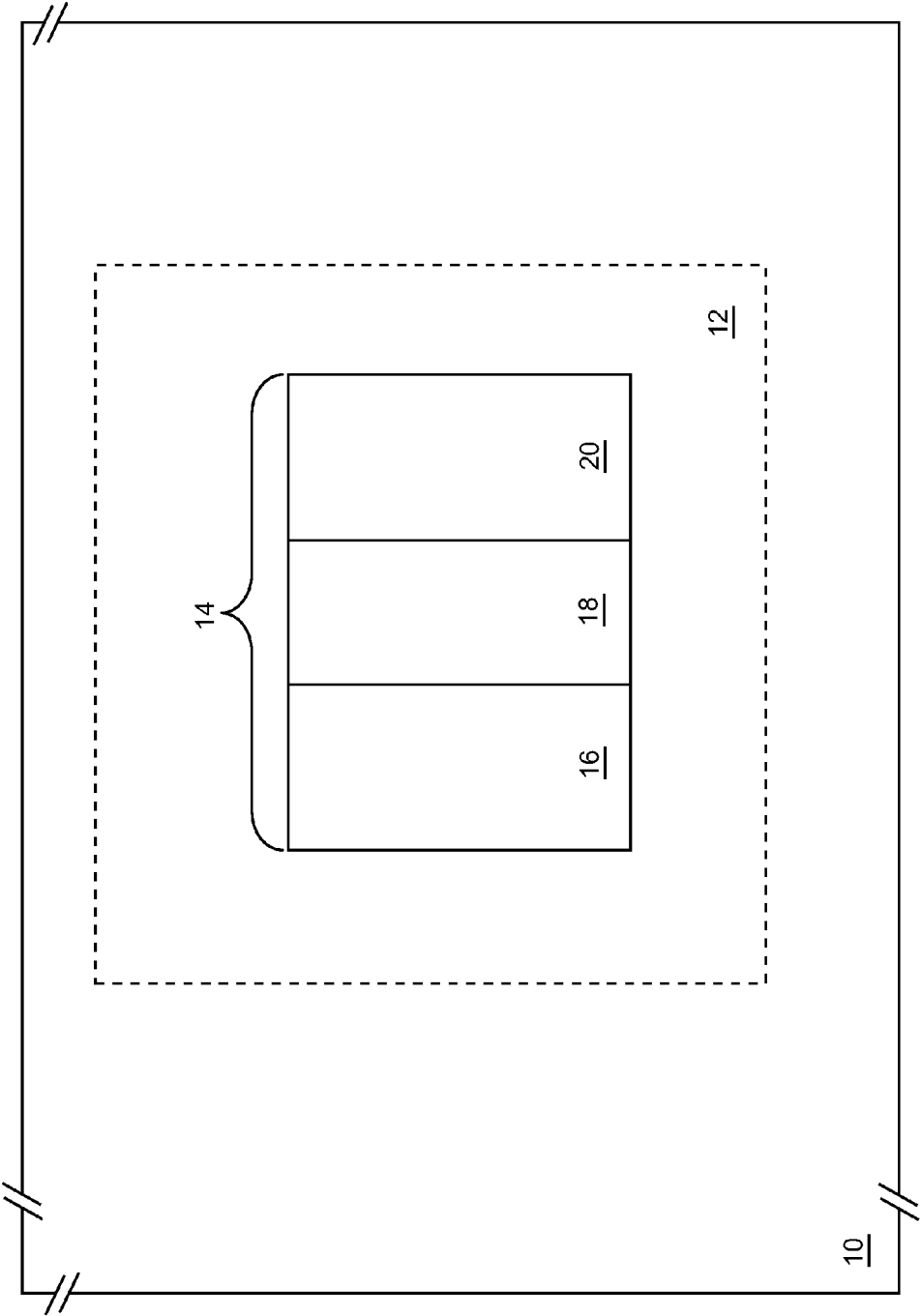


FIG. 1
PRIOR ART

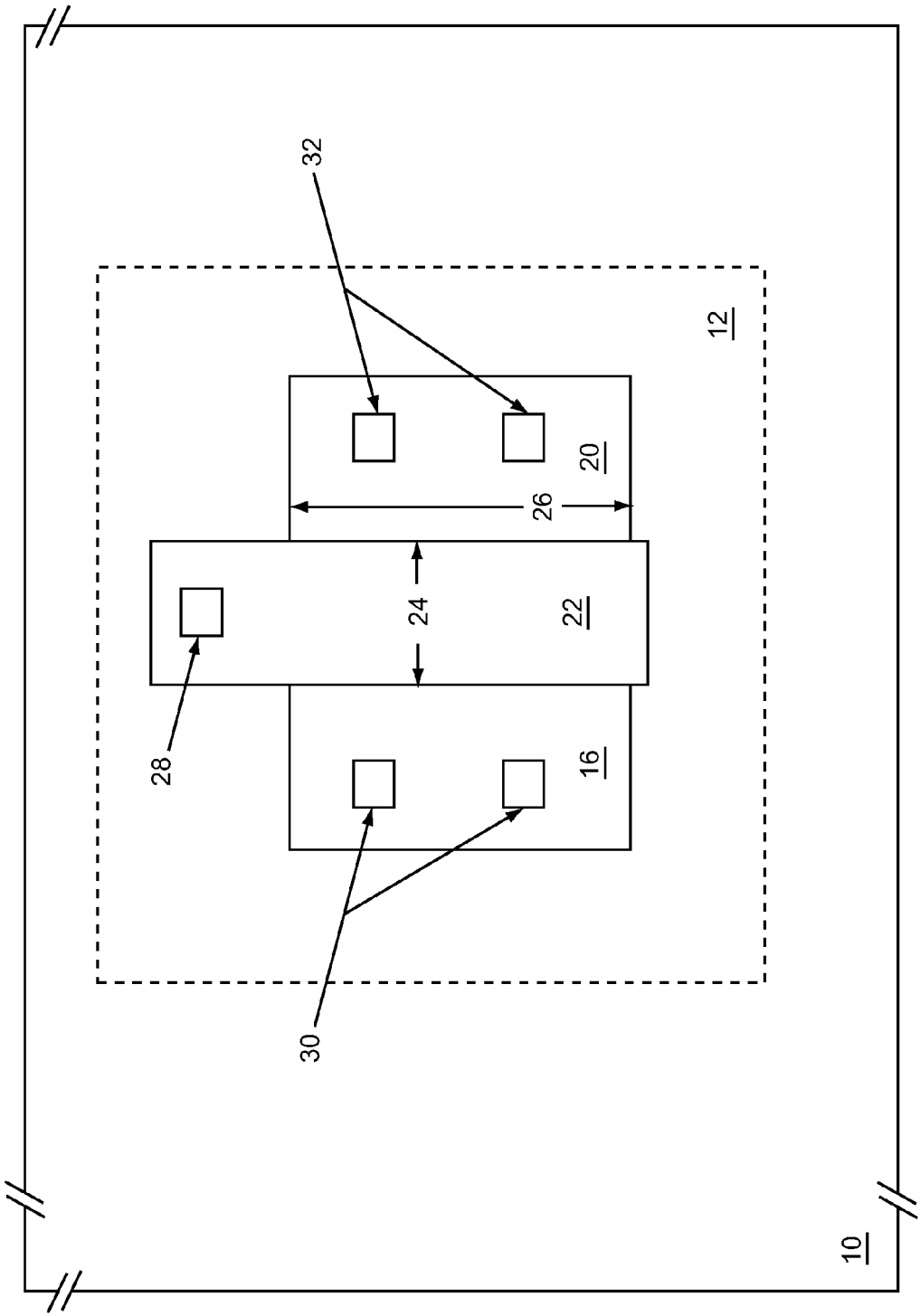


FIG. 2
PRIOR ART

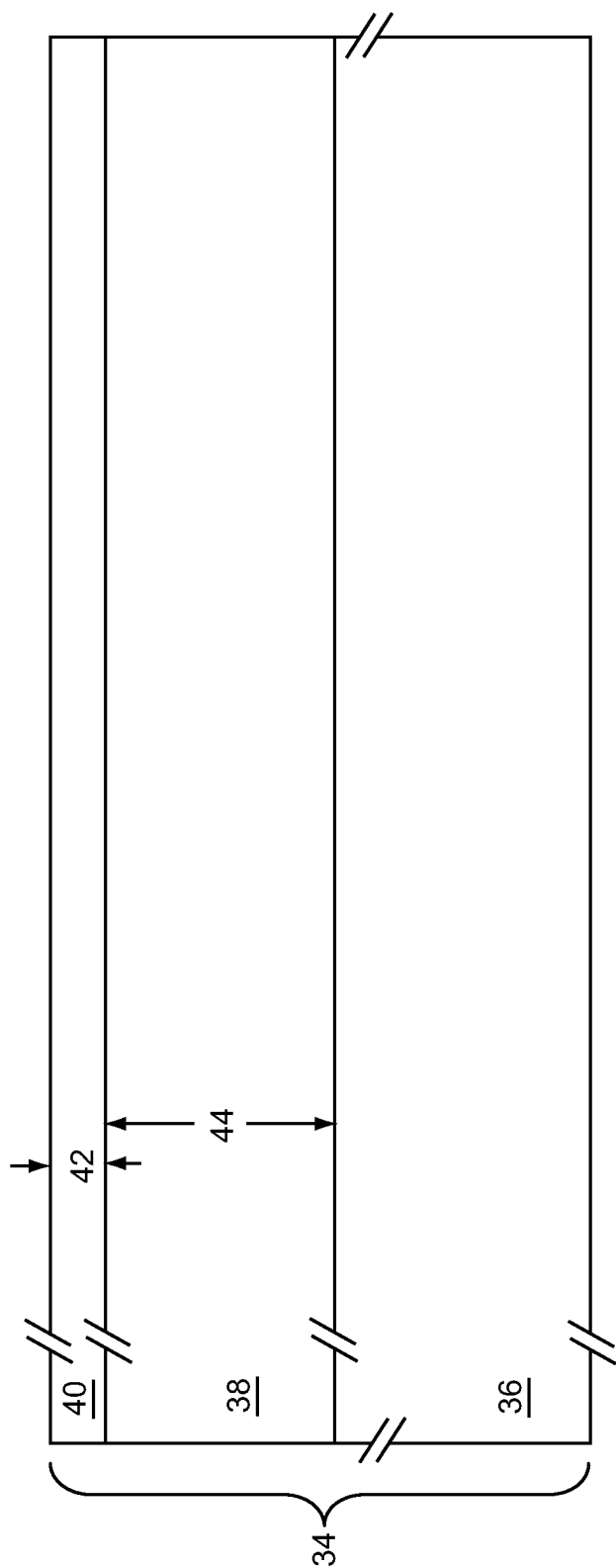


FIG. 3

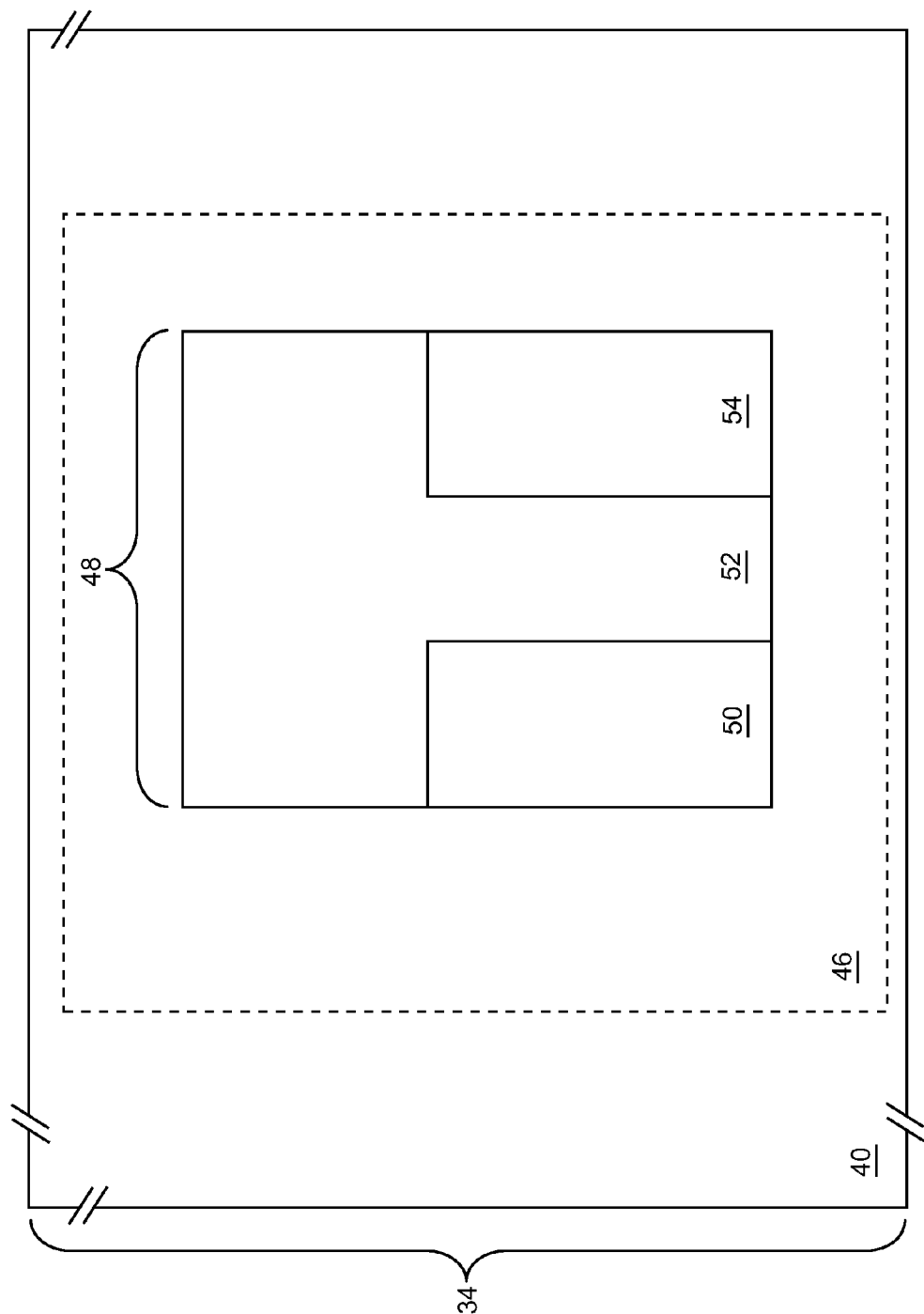


FIG. 4

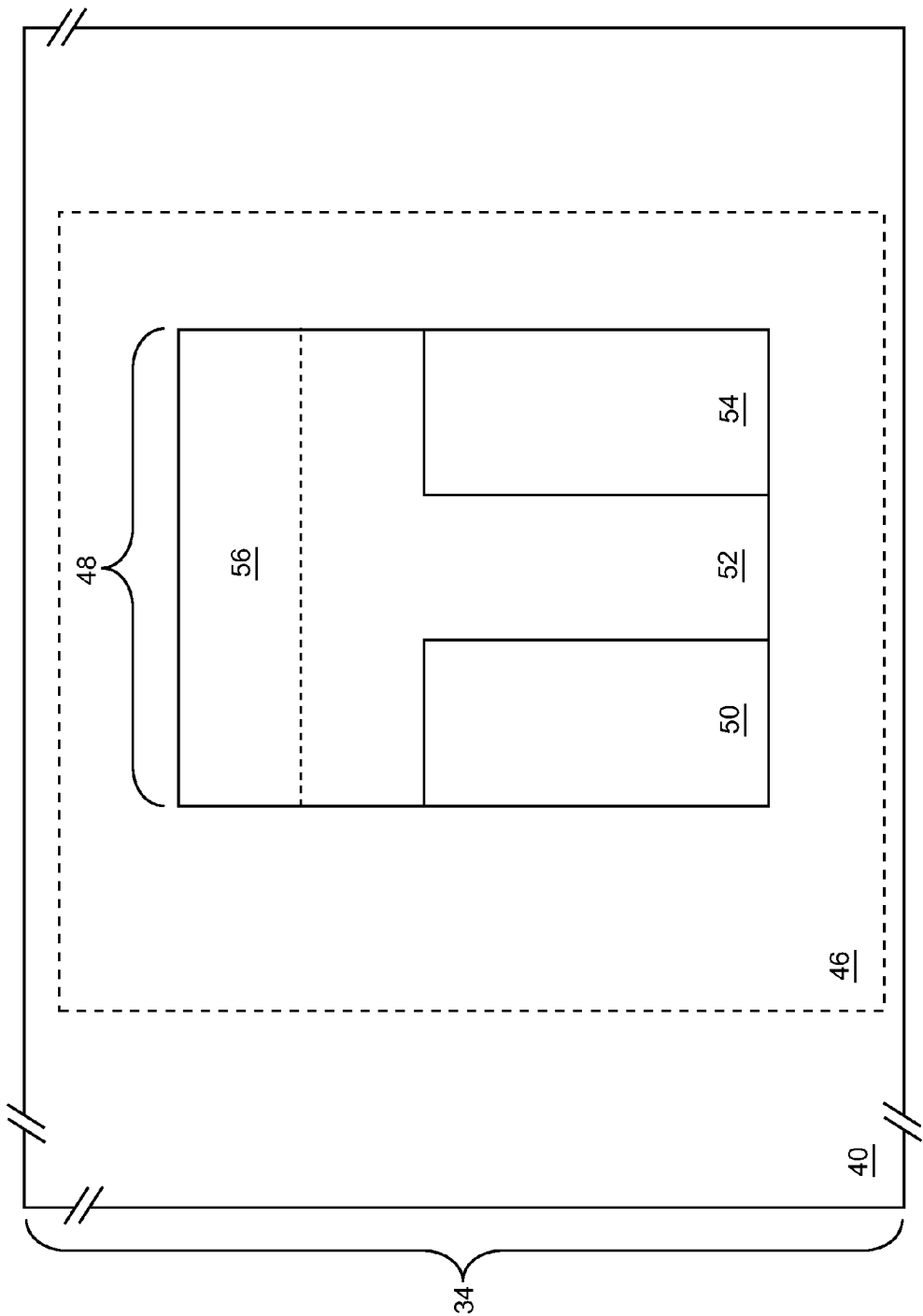


FIG. 5

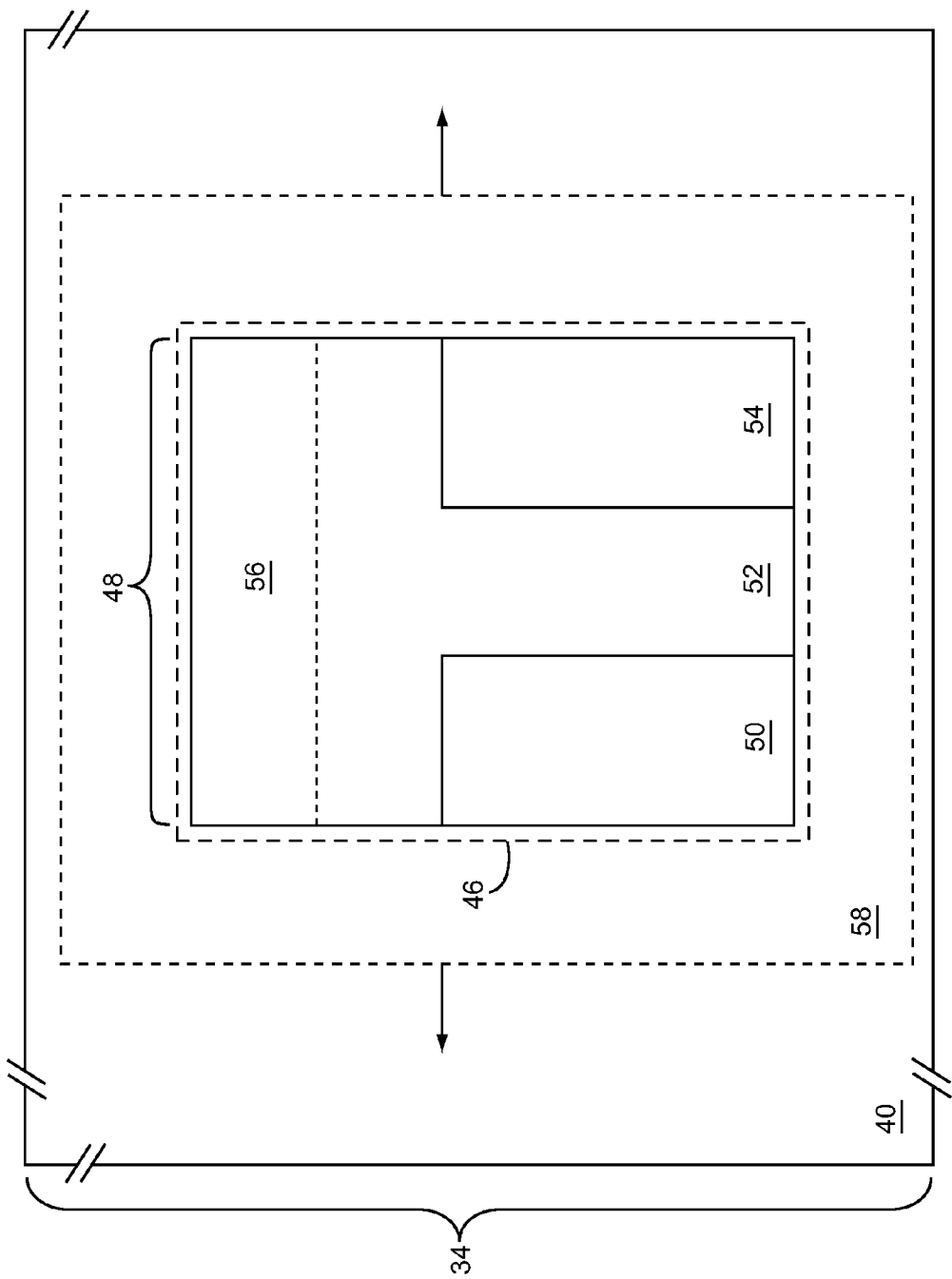
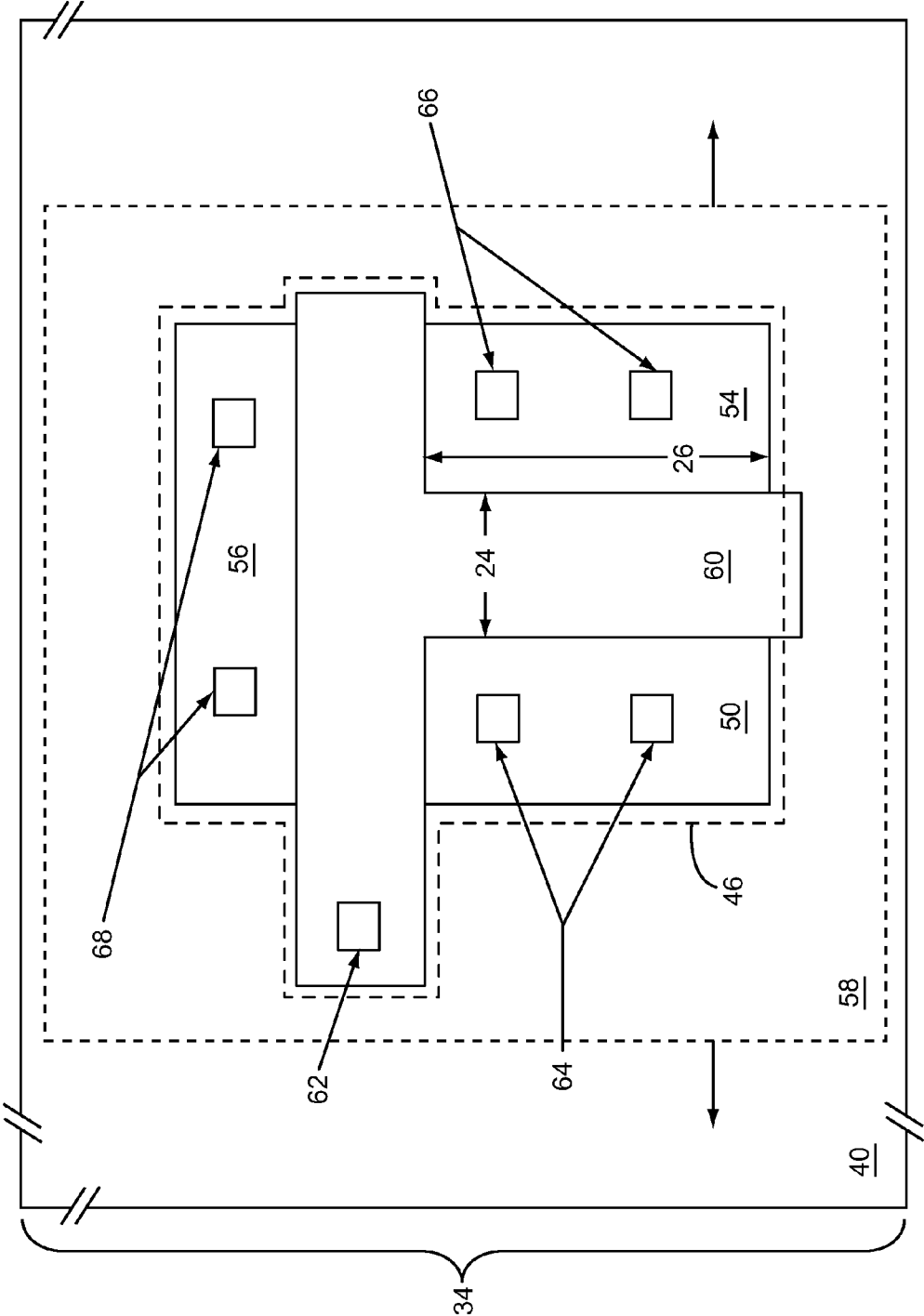


FIG. 6



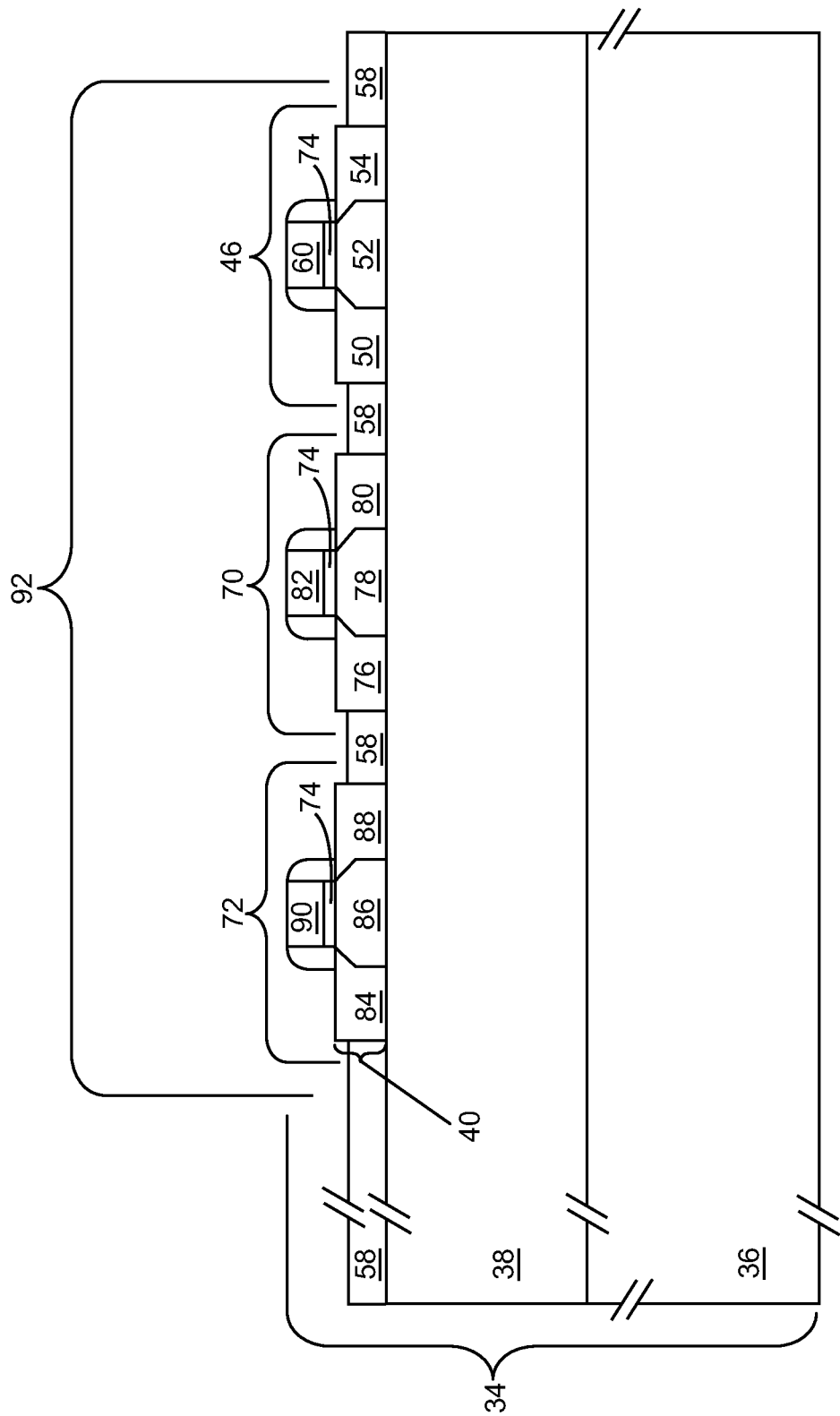


FIG. 8

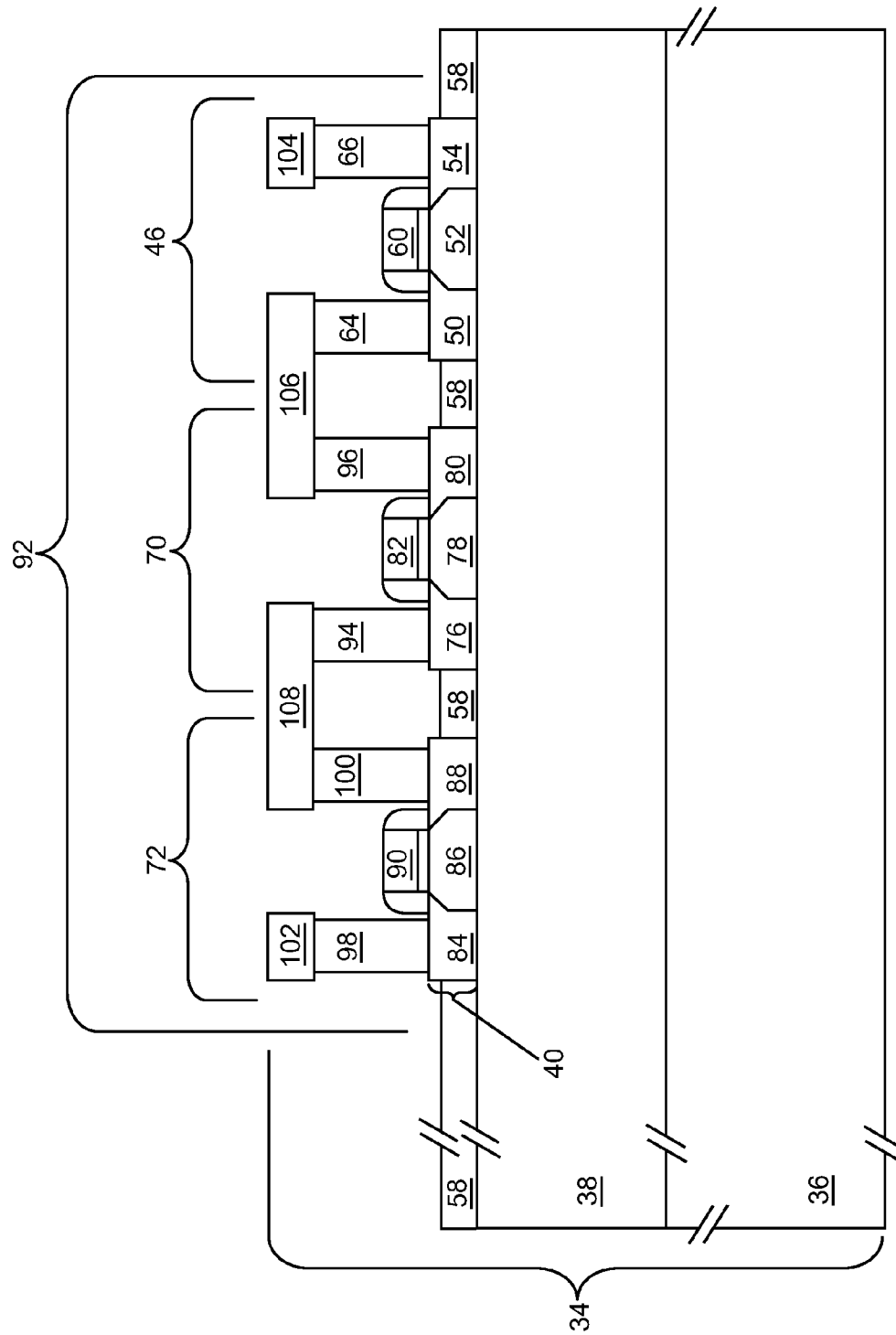


FIG. 9

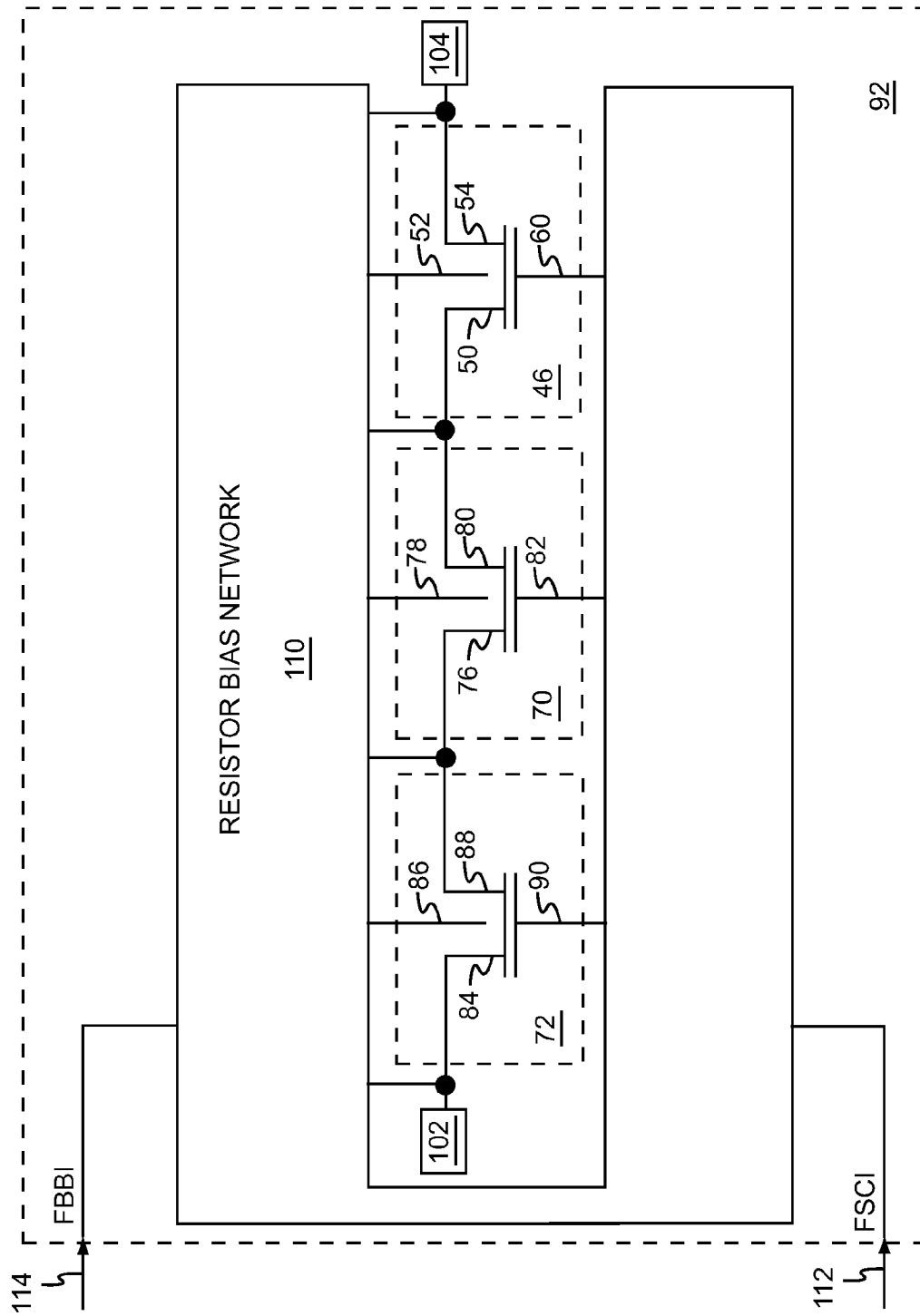


FIG. 10

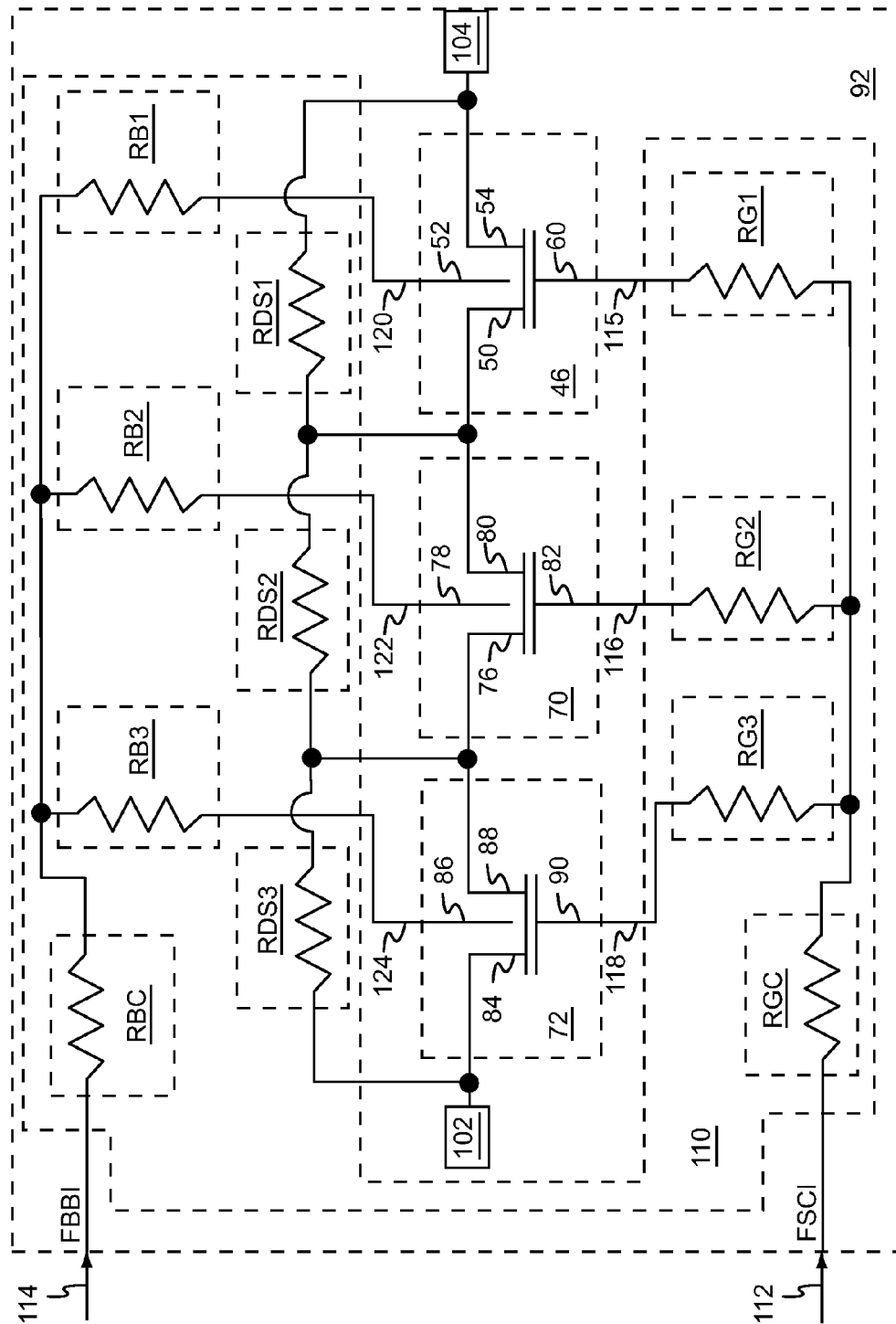


FIG. 11

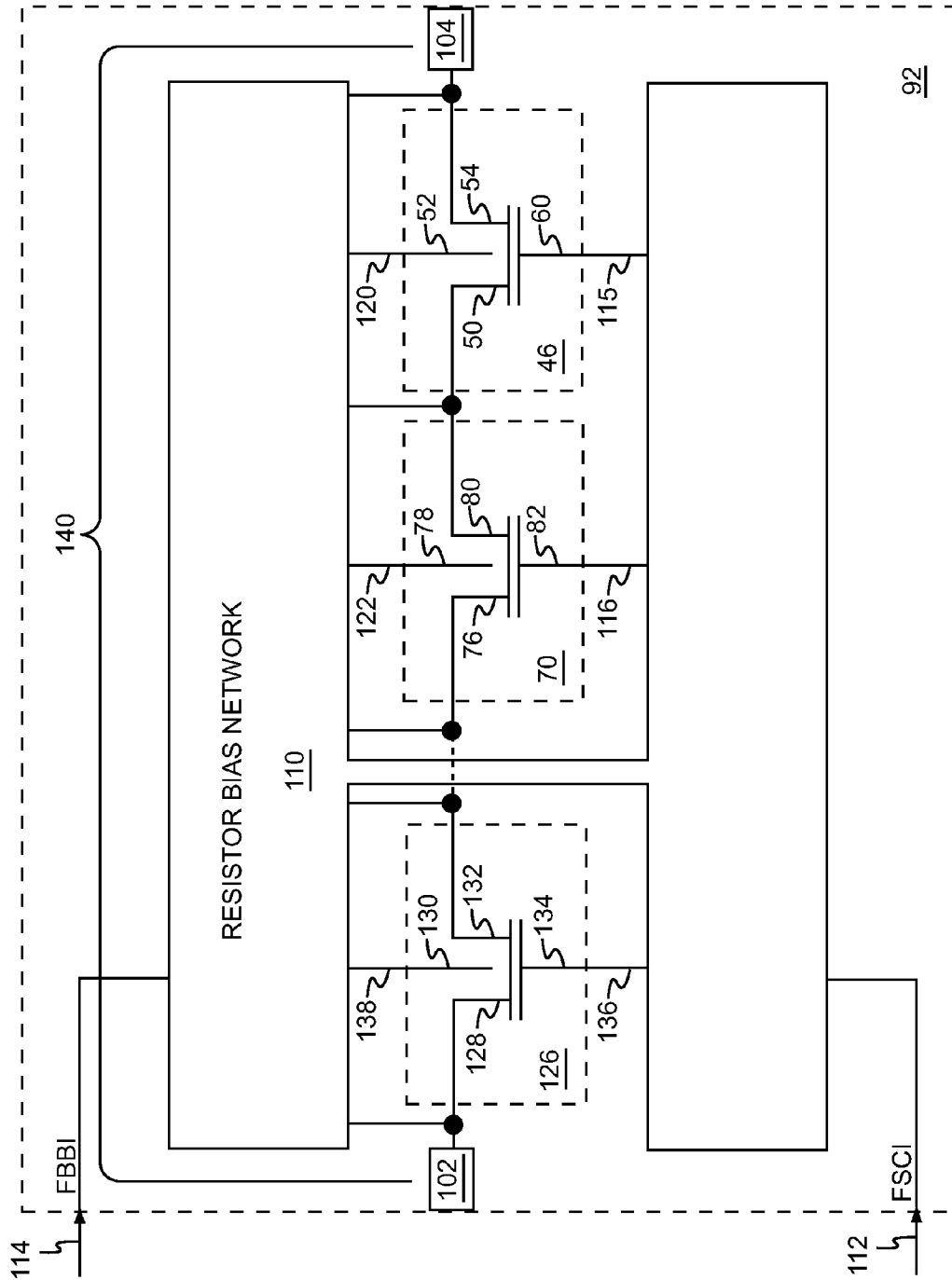


FIG. 12

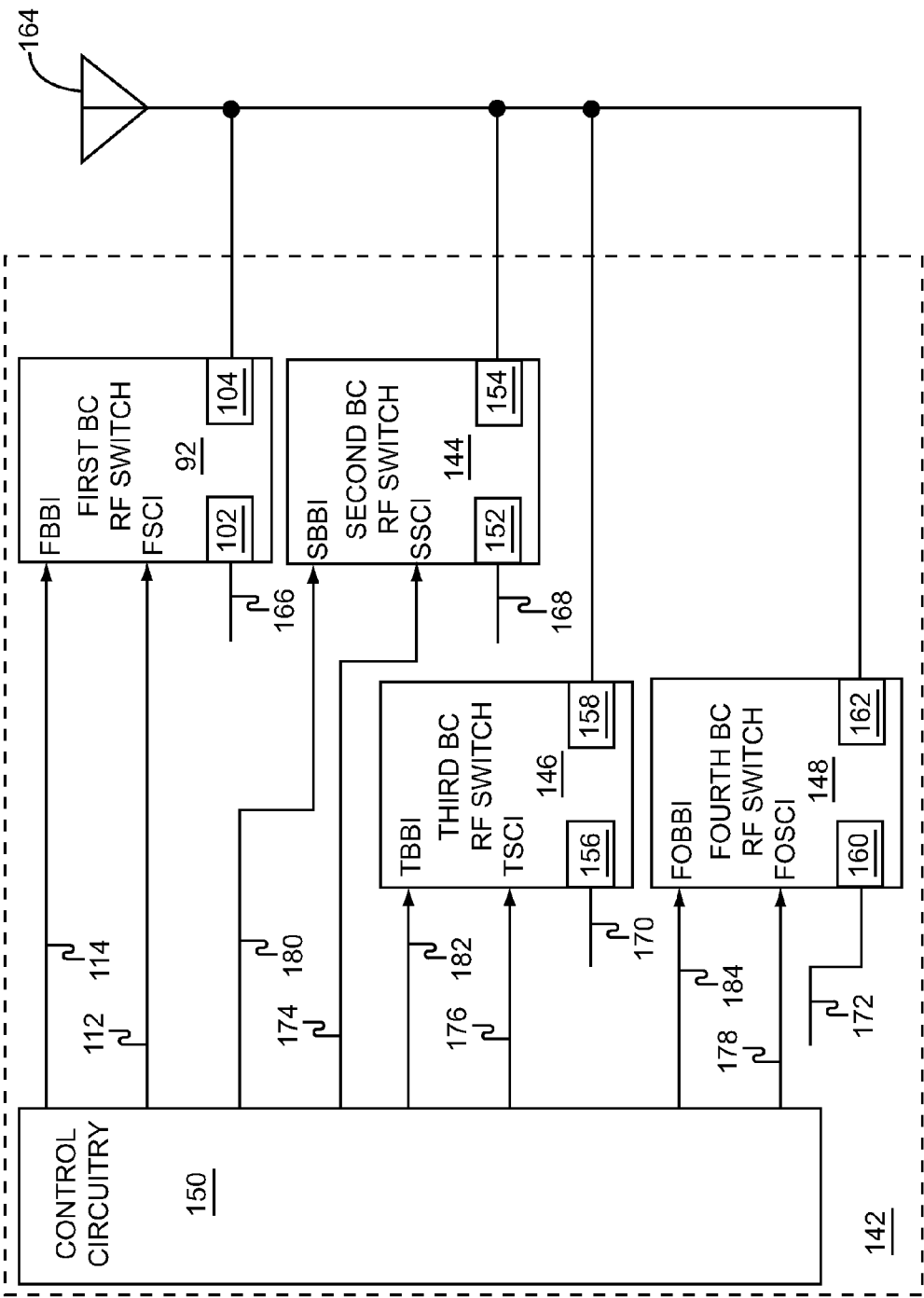


FIG. 13

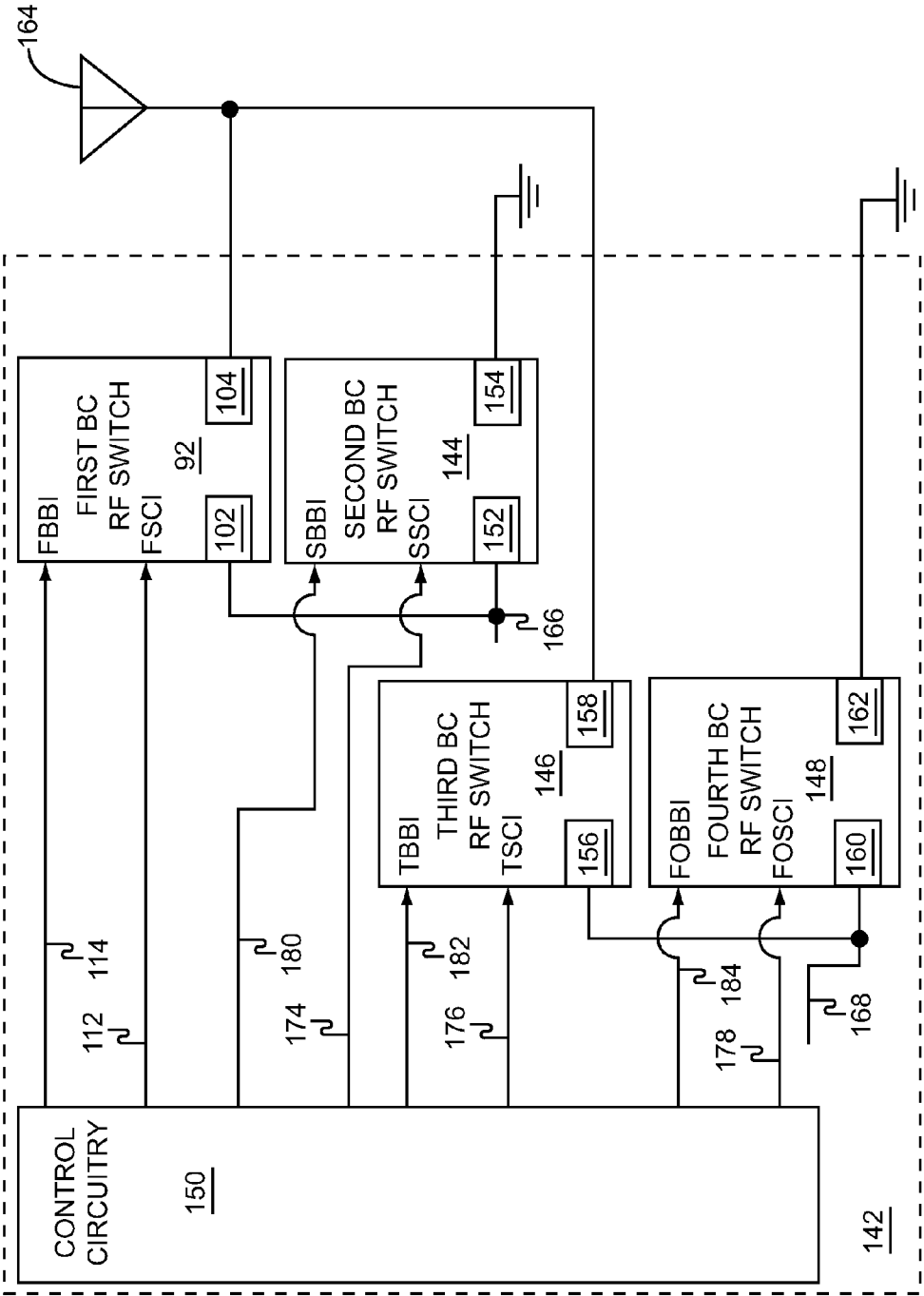


FIG. 14

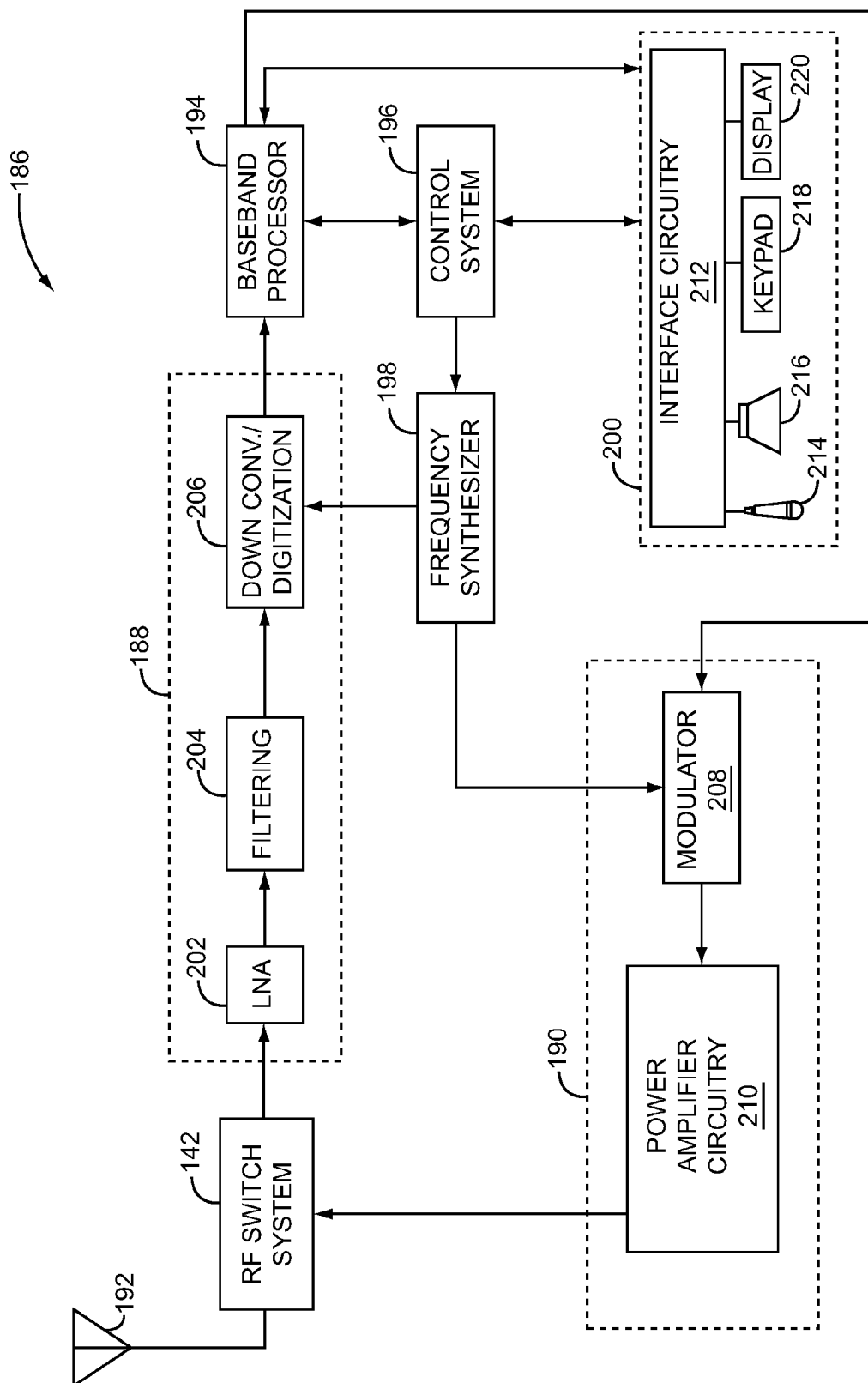


FIG. 15

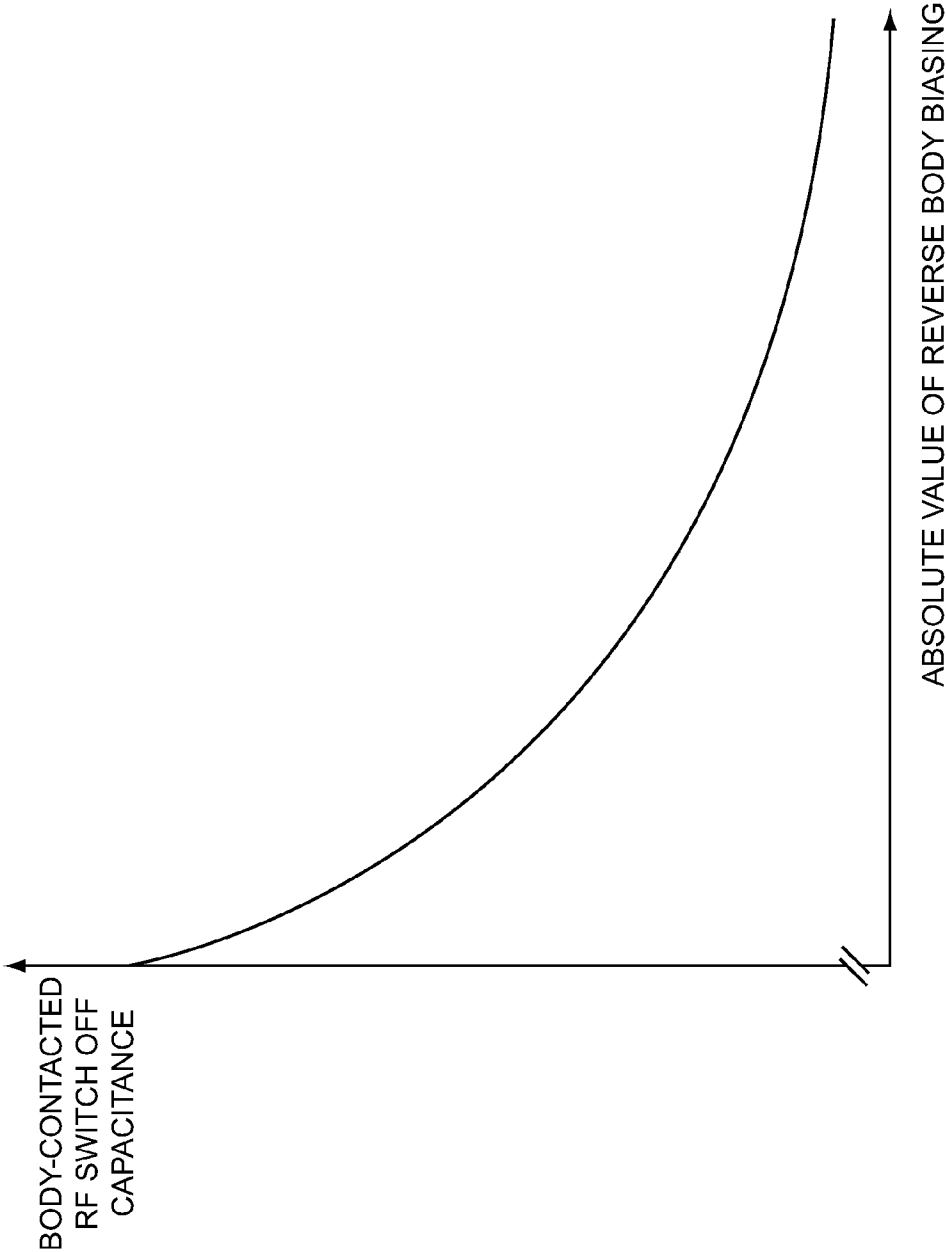
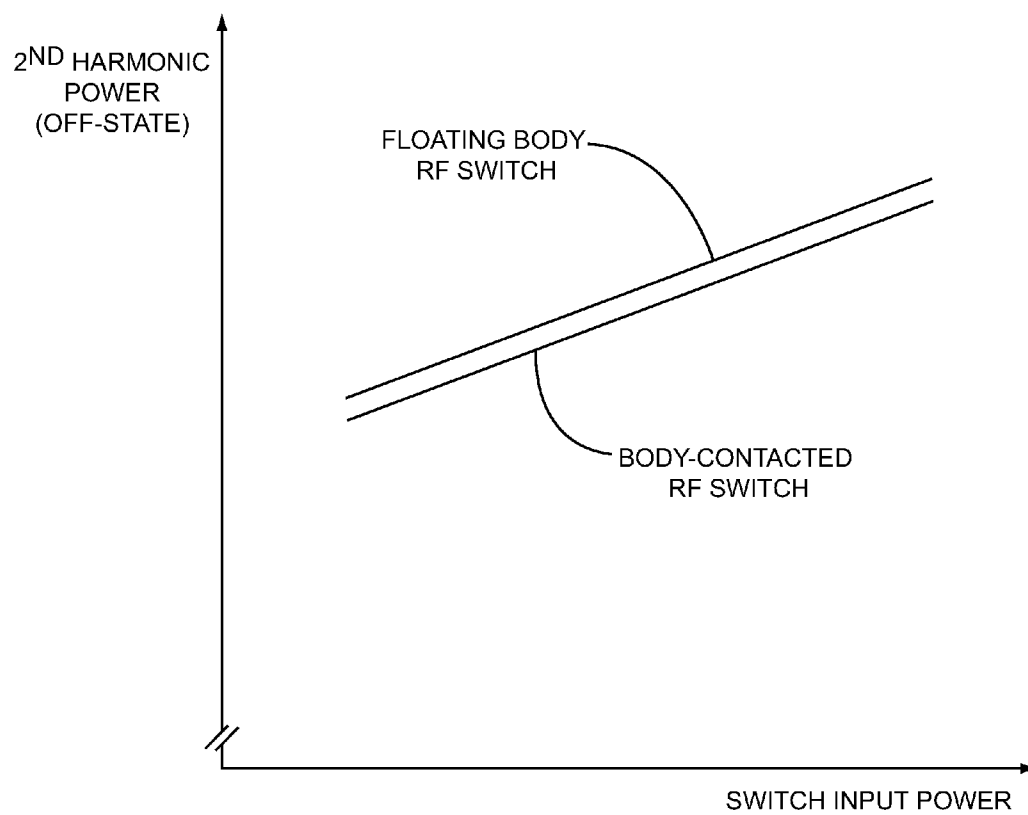
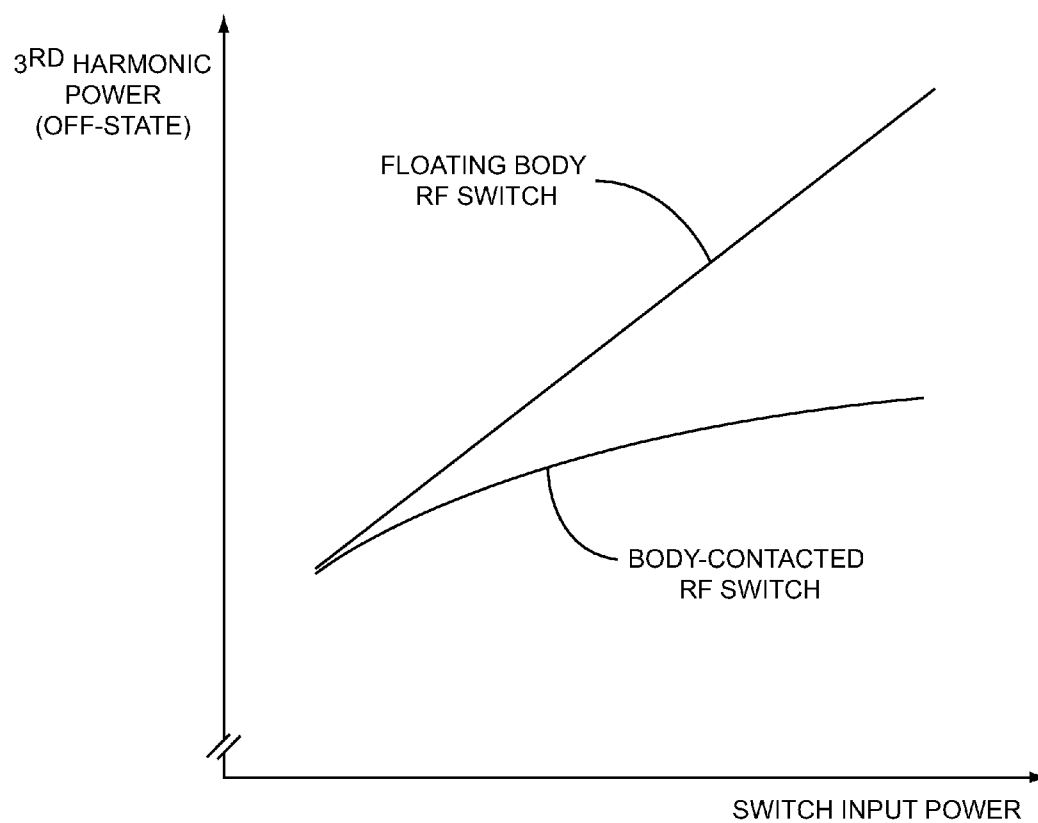


FIG. 16

*FIG. 17*

*FIG. 18*

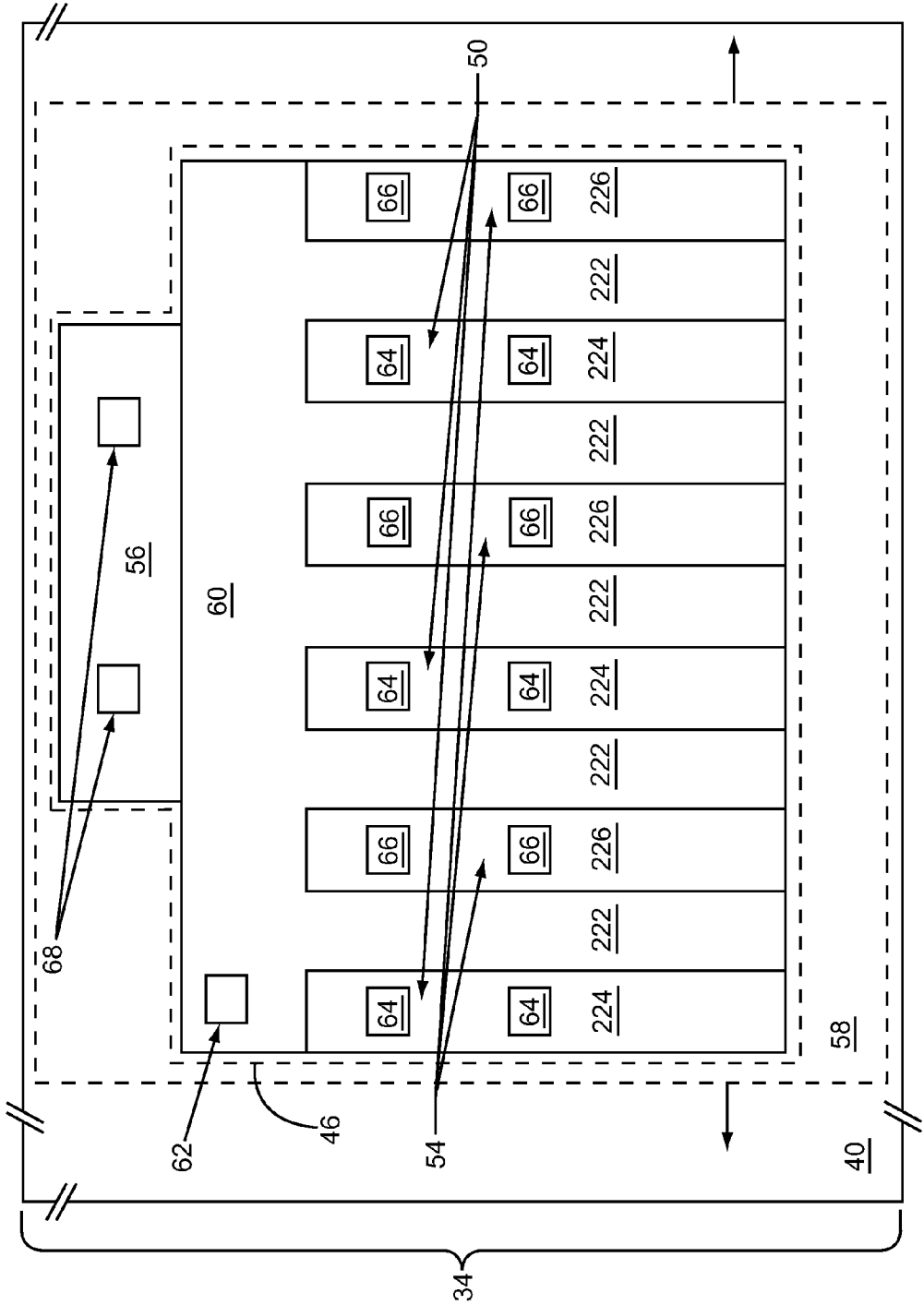


FIG. 19

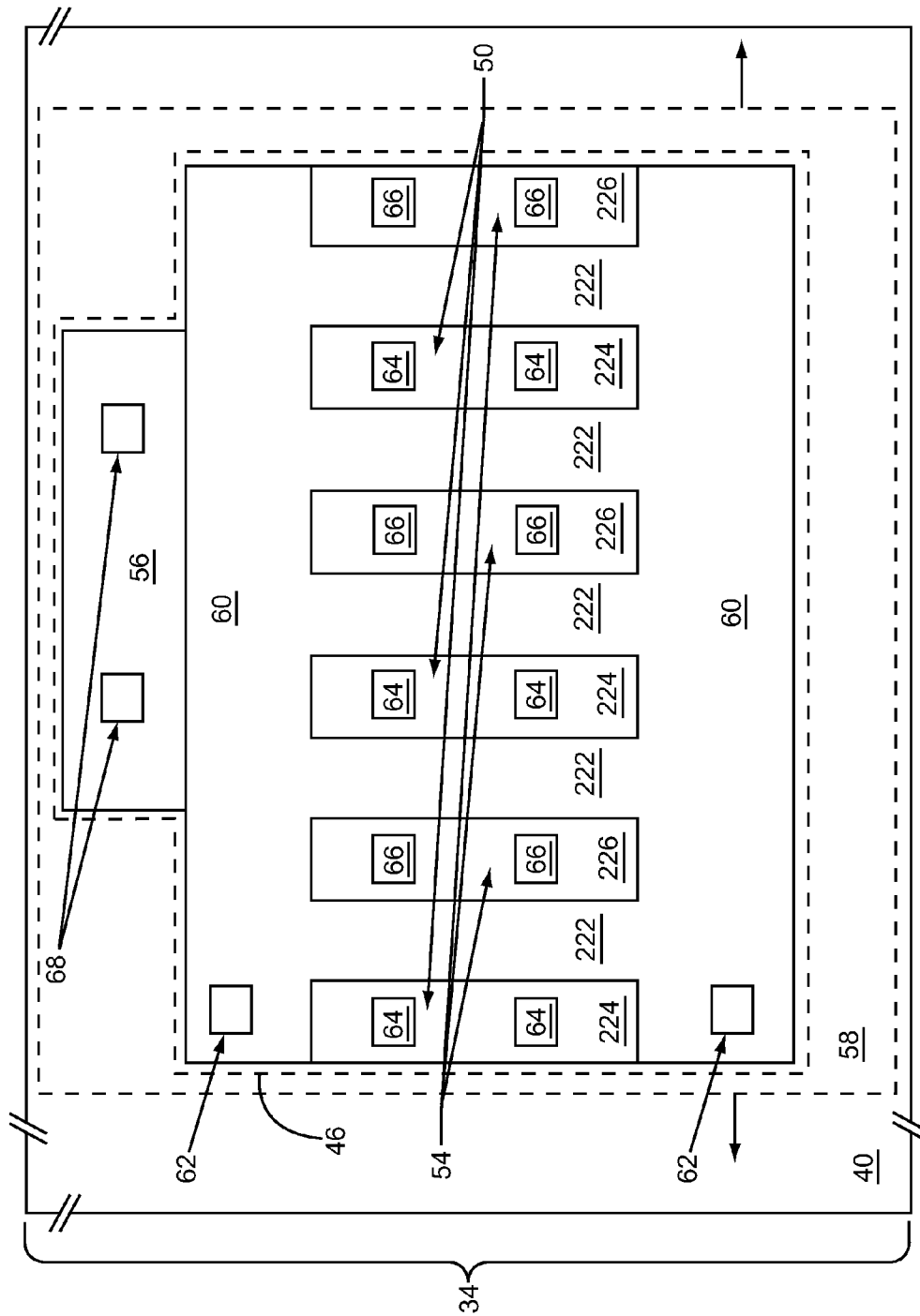


FIG. 20

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SEMICONDUCTOR RADIO FREQUENCY SWITCH WITH BODY CONTACT

This application claims the benefit of provisional patent application Ser. No. 61/159,668, filed Mar. 12, 2009, the disclosure of which is hereby incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

Embodiments of the present disclosure relate to semiconductor and silicon-on-insulator (SOI) technologies and semiconductor-based radio frequency (RF) switches, both of which may be used in RF communications circuits.

BACKGROUND OF THE DISCLOSURE

As technology progresses, wireless communications devices, such as smart phones, wireless capable computers, or the like, are becoming increasingly integrated, feature rich, and complex. Such wireless communications devices rely on semiconductor technologies, such as silicon based technologies, which are evolving toward smaller circuit geometries, lower power consumption, higher operating speeds, and increased complexity. Complementary metal oxide semiconductor (CMOS) technology is an example of a silicon based technology. Further, wireless communications devices may need to support multiple communications bands, multiple communications modes, multiple communications protocols, and the like. As such, wireless communications devices may need multiple RF switches to select between different RF circuits depending on which communications bands, modes, and protocols are in use. Such complex RF systems may place strict linearity, insertion loss, and isolation demands on the RF switches.

In general, RF switches having semiconductor-based switching elements may have a trade-off between insertion loss and isolation. RF switches that must handle high power levels may require low insertion losses. In order to achieve low insertion loss and high power handling capability, the size of circuit elements within an RF switch may be relatively large. However, such large circuit elements may be associated with relatively large capacitances, which may decrease isolation. Further, multiple large capacitances may have non-linearities, which may degrade linearity of the RF switch. Thus, there is a need for a silicon based RF switch that improves the trade-off between insertion loss and isolation, has good linearity performance, operates over multiple frequency bands, or any combination thereof.

SUMMARY OF THE EMBODIMENTS

The present disclosure relates to an RF switch that includes multiple body-contacted field effect transistor (FET) elements coupled in series. The FET elements may be formed using a thin-film semiconductor device layer, which is part of a thin-film semiconductor die. Conduction paths between the FET elements through the thin-film semiconductor device layer and through a substrate of the thin-film semiconductor die may be substantially eliminated by using insulating materials. Elimination of the conduction paths allows an RF signal across the RF switch to be divided across the series coupled FET elements, such that each FET element is subjected to only a portion of the RF signal. Further, each FET element is body-contacted and may receive reverse body biasing when the RF switch is in an OFF state, thereby reducing an OFF state drain-to-source capacitance of each FET element. The

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combination of dividing the RF signal and reverse body biasing each FET element when the RF switch is in an OFF state may improve the trade-off between insertion loss and isolation, may improve linearity performance, and may enable the RF switch to operate over multiple frequency bands.

Thin-film semiconductor dies may typically be used in conjunction with complementary metal oxide semiconductor (CMOS) processes, which may be used to fabricate high performance microprocessors due to comparatively low source-to-body and drain-to-body junction capacitances. However, low source-to-body and drain-to-body junction capacitances may be beneficial in certain RF circuits, such as RF switches. Low source-to-body and drain-to-body junction capacitances may provide a low OFF state drain-to-source capacitance of an FET element. Further, by using insulating materials to completely surround each FET element in the RF switch, a body, a source, and a drain of each FET element may be isolated from the substrate and may be isolated from other devices, including other FET elements, via the thin-film semiconductor device layer.

During the OFF state of the RF switch, a voltage may be applied between the body and the source of each FET element to reverse bias the body and the source, and a voltage may be applied between the body and the drain of each FET element to reverse bias the body and the drain to body-contact and reverse body bias the FET element. By reverse biasing the body and the source, the source-to-body junction capacitance may be further reduced, and by reverse biasing the body and the drain, the drain-to-body junction capacitance may be further reduced, thereby further reducing the OFF state drain-to-source capacitance of each FET element. Such junction capacitance reductions may further improve the trade-off between insertion loss and isolation, may further improve linearity performance, and may further enable the RF switch to operate over multiple frequency bands. The improved linearity performance of the RF switch may be based on reduced harmonic distortion of the RF switch or reduced intermodulation distortion.

In addition, for CMOS processes, maximum drain-to-source voltage ratings may be between about one volt and about five volts, depending on the technology. However, the RF signal across the RF switch when the RF switch is in the OFF state may be significantly larger than the maximum drain-to-source voltage ratings. Therefore, the RF switch may include multiple body-contacted FET elements coupled in series to divide the RF signal across the series-coupled FET elements. The division of the RF signal needs to be reasonably balanced during the OFF state and during transitions between the OFF state and an ON state to avoid exceeding maximum drain-to-source voltage ratings. As mentioned above, conduction paths between the FET elements through the thin-film semiconductor device layer and through the substrate of the thin-film semiconductor die may be substantially eliminated by using insulating materials, thereby helping to avoid exceeding maximum drain-to-source voltage ratings.

Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of

the disclosure, and together with the description serve to explain the principles of the disclosure.

FIG. 1 shows a top view of a conventional substrate, which is used to form a floating-body field effect transistor (FET) element according to the prior art.

FIG. 2 shows a top view of details of the floating-body FET element illustrated in FIG. 1 according to the prior art.

FIG. 3 shows a cross-section of a thin-film semiconductor die according to one embodiment of the thin-film semiconductor die.

FIG. 4 shows a top view of a first body-contacted FET element formed using the thin-film semiconductor die illustrated in FIG. 3 according to one embodiment of the first body-contacted FET element.

FIG. 5 shows a top view of details of the first body-contacted FET element illustrated in FIG. 4 according to an alternate embodiment of the first body-contacted FET element.

FIG. 6 shows a top view of details of the first body-contacted FET element illustrated in FIG. 5 according to an additional embodiment of the first body-contacted FET element.

FIG. 7 shows a top view of details of the first body-contacted FET element illustrated in FIG. 4 according to another embodiment of the first body-contacted FET element.

FIG. 8 shows a cross-section of the thin-film semiconductor die according to an alternate embodiment of the thin-film semiconductor die.

FIG. 9 shows a cross-section of the thin-film semiconductor die according to an additional embodiment of the thin-film semiconductor die.

FIG. 10 is a schematic diagram showing the first body-contacted RF switch illustrated in FIG. 9 according to one embodiment of the first body-contacted RF switch.

FIG. 11 is a schematic diagram showing details of a resistor bias network illustrated in FIG. 10 according to one embodiment of the resistor bias network.

FIG. 12 is a schematic diagram showing the first body-contacted RF switch according to an alternate embodiment of the first body-contacted RF switch.

FIG. 13 shows an RF switch system according to one embodiment of the RF switch system.

FIG. 14 shows the RF switch system according to an alternate embodiment of the RF switch system.

FIG. 15 shows an application example of the present disclosure used in a mobile terminal.

FIG. 16 is a graph illustrating a relationship between a body-contacted RF switch OFF capacitance of the first body-contacted RF switch and an absolute value of reverse body biasing of the first body-contacted RF switch.

FIG. 17 is a graph illustrating a relationship between second harmonic power of both floating-body and body-contacted RF switches in an OFF state and input power to the RF switches.

FIG. 18 is a graph illustrating a relationship between third harmonic power of both floating-body and body-contacted RF switches in an OFF state and input power to the RF switches.

FIG. 19 shows a top view of details of the first body-contacted FET element illustrated in FIG. 4 according to one embodiment of the first body-contacted FET element.

FIG. 20 shows a top view of details of the first body-contacted FET element illustrated in FIG. 4 according to an alternate embodiment of the first body-contacted FET element.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the disclosure and illustrate the best mode of practicing the disclosure. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

The present disclosure relates to an RF switch that includes multiple body-contacted field effect transistor (FET) elements coupled in series. The FET elements may be formed using a thin-film semiconductor device layer, which is part of a thin-film semiconductor die. Conduction paths between the FET elements through the thin-film semiconductor device layer and through a substrate of the thin-film semiconductor die may be substantially eliminated by using insulating materials. Elimination of the conduction paths allows an RF signal across the RF switch to be divided across the series coupled FET elements, such that each FET element is subjected to only a portion of the RF signal. Further, each FET element is body-contacted and may receive reverse body biasing when the RF switch is in an OFF state, thereby reducing an OFF state drain-to-source capacitance of each FET element. The combination of dividing the RF signal and reverse body biasing each FET element when the RF switch is in an OFF state may improve the trade-off between insertion loss and isolation, may improve linearity performance, and may enable the RF switch to operate over multiple frequency bands.

Thin-film semiconductor dies may typically be used in conjunction with complementary metal oxide semiconductor (CMOS) processes, which may be used to fabricate high performance microprocessors due to comparatively low source-to-body and drain-to-body junction capacitances. However, low source-to-body and drain-to-body junction capacitances may be beneficial in certain RF circuits, such as RF switches. Low source-to-body and drain-to-body junction capacitances may provide a low OFF state drain-to-source capacitance of an FET element. Further, by using insulating materials to completely surround each FET element in the RF switch, a body, a source, and a drain of each FET element may be isolated from the substrate and may be isolated from other devices, including other FET elements, via the thin-film semiconductor device layer.

Reverse bias of a PN junction occurs when a positive voltage is applied to the N-type material relative to the P-type material and a magnitude of the positive voltage is greater than zero. During the OFF state of the RF switch, a voltage may be applied between the body and the source of each FET element to reverse bias the body and the source, and a voltage may be applied between the body and the drain of each FET element to reverse bias the body and the drain to body-contact and reverse body bias the FET element. By reverse biasing the body and the source, the source-to-body junction capacitance may be further reduced, and by reverse biasing the body and the drain, the drain-to-body junction capacitance may be further reduced, thereby further reducing the OFF state drain-to-source capacitance of each FET element. Such junction capacitance reductions may further improve the trade-off between insertion loss and isolation, may further improve linearity performance, and may further enable the RF switch to operate over multiple frequency bands. The improved lin-

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earity performance of the RF switch may be based on reduced harmonic distortion of the RF switch.

In addition, for CMOS processes, maximum drain-to-source voltage ratings may be between about one volt and about five volts, depending on the technology. However, the RF signal across the RF switch when the RF switch is in the OFF state may be significantly larger than the maximum drain-to-source voltage ratings. Therefore, the RF switch may include multiple body-contacted FET elements coupled in series to divide the RF signal across the series-coupled FET elements. The division of the RF signal needs to be reasonably balanced during the OFF state and during transitions between the OFF state and an ON state to avoid exceeding maximum drain-to-source voltage ratings. As mentioned above, conduction paths between the FET elements through the thin-film semiconductor device layer and through the substrate of the thin-film semiconductor die may be substantially eliminated by using insulating materials, thereby helping to avoid exceeding maximum drain-to-source voltage ratings.

FIG. 1 shows a top view of a conventional substrate 10, which is used to form a floating-body FET element 12 according to the prior art. The floating-body FET element 12 includes an active region 14, which is formed in the conventional substrate 10. The active region 14 includes a conventional source 16, a floating body 18, and a conventional drain 20. The floating body 18 is between the conventional source 16 and the conventional drain 20 and provides a channel for the floating-body FET element 12. In one configuration, the conventional source 16 and the conventional drain 20 include N-type semiconductor material, and the floating body 18 includes P-type semiconductor material. In an alternate configuration, the conventional source 16 and the conventional drain 20 include P-type semiconductor material, and the floating body 18 includes N-type semiconductor material.

FIG. 2 shows a top view of details of the floating-body FET element 12 illustrated in FIG. 1 according to the prior art. The floating-body FET element 12 includes a conventional gate 22 over the conventional substrate 10. The conventional gate 22 has a gate length 24 and a gate width 26 over the channel of the floating-body FET element 12. Further, the conventional gate 22 may completely cover the floating body 18 as shown. The conventional gate 22 may have a gate contact 28, the conventional source 16 may have source contacts 30, and the conventional drain 20 may have drain contacts 32. The gate, the source, and the drain contacts 28, 30, 32 provide electrical connectivity to the conventional gate 22, the conventional source 16, and the conventional drain 20, respectively. The floating body 18 has no electrical contacts and is electrically coupled to other devices only through the conventional substrate 10, the conventional gate 22, the conventional source 16, the conventional drain 20, or any combination thereof.

FIG. 3 shows a cross-section of a thin-film semiconductor die 34, which may be a thin-film silicon-on-insulator (SOI) semiconductor die, according to one embodiment of the thin-film semiconductor die 34. The thin-film semiconductor die 34 includes a substrate 36, which may be an SOI substrate; an insulating layer 38, which may be an SOI insulating layer, over the substrate 36; and a thin-film semiconductor device layer 40, which may be a thin-film SOI device layer, over the insulating layer 38. The thin-film semiconductor device layer 40 has a semiconductor device layer thickness 42 and the insulating layer 38 has an insulating layer thickness 44. The substrate 36 may include silicon, sapphire, other semiconductor material, insulating material, or any combination thereof. The substrate 36 may be provided from a silicon handle wafer.

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The insulating layer 38 may include oxide, buried oxide, silicon dioxide, other insulating material, or any combination thereof. The thin-film semiconductor device layer 40 is a thin-film layer that includes silicon and is used to form electronic devices, such as transistor elements, diode elements, resistive elements, capacitive elements, or the like. The insulating layer 38 may be used to electrically isolate the thin-film semiconductor device layer 40 from the substrate 36.

In one embodiment of the thin-film semiconductor device layer 40, the thin-film semiconductor device layer 40 is partially-depleted SOI and not fully-depleted SOI. As the insulating layer thickness 44 increases, RF coupling to adjacent devices through the substrate 36 may be reduced, thereby improving isolation. Additionally, as resistivity of the substrate 36 increases, RF coupling to adjacent devices may be reduced, thereby improving RF performance of active RF devices and passive RF devices, such as inductors and transmission lines.

In a first exemplary embodiment of the substrate 36, the resistivity of the substrate 36 is greater than about 100 ohm-centimeters. In a second exemplary embodiment of the substrate 36, the resistivity of the substrate 36 is greater than about 500 ohm-centimeters. In a third exemplary embodiment of the substrate 36, the resistivity of the substrate 36 is greater than about 1000 ohm-centimeters. In one embodiment of the thin-film semiconductor die 34, the insulating layer thickness 44 is greater than the semiconductor device layer thickness 42. In a first exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is between about 100 nanometers and about 300 nanometers. In a second exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 900 nanometers. In a third exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 700 nanometers. In a fourth exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 500 nanometers. In a fifth exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 300 nanometers. In a sixth exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 200 nanometers. In a seventh exemplary embodiment of the thin-film semiconductor device layer 40, the semiconductor device layer thickness 42 is less than about 100 nanometers.

In a first exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is between about 200 nanometers and about 1000 nanometers. In a second exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is greater than about 200 nanometers. In a third exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is greater than about 600 nanometers. In a fourth exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is greater than about 1000 nanometers. In a fifth exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is greater than about 1500 nanometers. In a sixth exemplary embodiment of the insulating layer 38, the insulating layer thickness 44 is greater than about 2000 nanometers.

FIG. 4 shows a top view of a first body-contacted FET element 46 formed using the thin-film semiconductor die 34 illustrated in FIG. 3 according to one embodiment of the first body-contacted FET element 46. The first body-contacted FET element 46 includes an active region 48, which is formed in the thin-film semiconductor device layer 40. The active

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region 48 includes a first source 50, a first body 52, and a first drain 54. The first body 52 is between the first source 50 and the first drain 54 and provides a channel for the first body-contacted FET element 46. Either or both of the first source 50 and the first drain 54 may include heavily doped semiconductor material to increase connectivity and provide one or more regions for making electrical connections to the first source 50 and the first drain 54, respectively.

In a first exemplary embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include N-type semiconductor material, and the first body 52 includes P-type semiconductor material. In a second exemplary embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include heavily doped N-type semiconductor material, and the first body 52 includes P-type semiconductor material. In a third exemplary embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include P-type semiconductor material, and the first body 52 includes N-type semiconductor material. In a fourth exemplary embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include heavily doped P-type semiconductor material, and the first body 52 includes N-type semiconductor material.

FIG. 5 shows a top view of details of the first body-contacted FET element 46 illustrated in FIG. 4 according to an alternate embodiment of the first body-contacted FET element 46. The first body 52 of the first body-contacted FET element 46 includes a first body contact region 56, which may include heavily doped semiconductor material to increase connectivity and provide one or more regions for making electrical connections to the first body 52. In a first exemplary embodiment of the first body 52, the first body 52 includes P-type semiconductor material and the first body contact region 56 includes heavily doped P-type semiconductor material. In a second exemplary embodiment of the first body 52, the first body 52 includes N-type semiconductor material and the first body contact region 56 includes heavily doped N-type semiconductor material.

FIG. 6 shows a top view of details of the first body-contacted FET element 46 illustrated in FIG. 5 according to an additional embodiment of the first body-contacted FET element 46. The first body-contacted FET element 46 includes insulating material 58 in the thin-film semiconductor device layer 40 and may completely surround the active region 48. Completely surrounding the active region 48 with the insulating material 58 may substantially eliminate conduction paths between the first body-contacted FET element 46 and other devices through the thin-film semiconductor device layer 40. In general, in thin-film semiconductor processing, all regions outside of the active region 48 may be fully oxide isolated as part of the normal CMOS process. A CMOS shallow trench may be everywhere outside of active regions 48 and may extend down to the insulating layer 38 (FIG. 3).

FIG. 7 shows a top view of details of the first body-contacted FET element 46 illustrated in FIG. 4 according to another embodiment of the first body-contacted FET element 46. The first body-contacted FET element 46 includes a first gate 60 over the thin-film semiconductor device layer 40. The first gate 60 has the gate length 24 and the gate width 26 over the channel of the first body-contacted FET element 46. The first gate 60 may have a first gate contact 62, the first source 50 may have first source contacts 64, the first drain 54 may have first drain contacts 66, and the first body contact region 56 may have first body contacts 68. The first gate, the first source, the first drain, and the first body contacts 62, 64, 66, 68 may provide electrical connectivity to the first gate 60, the first

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source 50, the first drain 54, and the first body 52, respectively. The first gate 60 may extend over the insulating material 58, beyond the insulating material 58, or both. In one embodiment of the first gate 60, the first gate 60 includes polysilicon.

FIG. 8 shows a cross-section of the thin-film semiconductor die 34 illustrated in FIG. 3 according to an alternate embodiment of the thin-film semiconductor die 34. FIG. 8 shows a cross-section of the first body-contacted FET element 46, a second body-contacted FET element 70, and a third body-contacted FET element 72 formed using the thin-film semiconductor device layer 40. The first body-contacted FET element 46 includes the first source 50, the first body 52, the first drain 54, the insulating material 58, a gate oxide 74 over the first body 52, and the first gate 60 over the gate oxide 74. The first body 52 is between the first source 50 and the first drain 54, and the first source 50, the first body 52, and the first drain 54 are surrounded by the insulating material 58. The gate oxide 74 electrically insulates the first gate 60 from the first body 52. The first source 50, the first body 52, the first drain 54, or any combination thereof may completely traverse the semiconductor device layer thickness 42 (FIG. 3) of the thin-film semiconductor device layer 40. In one embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include N-type silicon, and the first body 52 includes P-type silicon. In an alternate embodiment of the first body-contacted FET element 46, the first source 50 and the first drain 54 include P-type silicon, and the first body 52 includes N-type silicon. Alternate embodiments of the first body-contacted FET element 46, the second body-contacted FET element 70, the third body-contacted FET element 72, the like, or any combination thereof may be formed using alternate layers, additional layers, or both having any type of implant or doping.

The second body-contacted FET element 70 may be similar to the first body-contacted FET element 46 and may include a second source 76, a second body 78, a second drain 80, the insulating material 58, the gate oxide 74 over the second body 78, and a second gate 82 over the gate oxide 74. The second body 78 is between the second source 76 and the second drain 80, and the second source 76, the second body 78, and the second drain 80 are surrounded by the insulating material 58. The gate oxide 74 electrically insulates the second gate 82 from the second body 78. The second body-contacted FET element 70 may include a second body contact region (not shown) and second body contacts (not shown). The second source 76, the second body 78, the second drain 80, or any combination thereof may completely traverse the semiconductor device layer thickness 42 (FIG. 3) of the thin-film semiconductor device layer 40. In one embodiment of the second body-contacted FET element 70, the second source 76 and the second drain 80 include N-type silicon, and the second body 78 includes P-type silicon. In an alternate embodiment of the second body-contacted FET element 70, the second source 76 and the second drain 80 include P-type silicon, and the second body 78 includes N-type silicon.

The third body-contacted FET element 72 may be similar to the first body-contacted FET element 46 and may include a third source 84, a third body 86, a third drain 88, the insulating material 58, the gate oxide 74 over the third body 86, and a third gate 90 over the gate oxide 74. The third body 86 is between the third source 84 and the third drain 88, and the third source 84, the third body 86, and the third drain 88 are surrounded by the insulating material 58. The gate oxide 74 electrically insulates the third gate 90 from the third body 86. The third body-contacted FET element 72 may include a third body contact region (not shown) and third body contacts

(not shown). The third source **84**, the third body **86**, the third drain **88**, or any combination thereof may completely traverse the semiconductor device layer thickness **42** (FIG. 3) of the thin-film semiconductor device layer **40**. In one embodiment of the third body-contacted FET element **72**, the third source **84** and the third drain **88** include N-type silicon, and the third body **86** includes P-type silicon. In an alternate embodiment of the third body-contacted FET element **72**, the third source **84** and the third drain **88** include P-type silicon, and the third body **86** includes N-type silicon.

A first body-contacted RF switch **92** includes the first body-contacted FET element **46**, the second body-contacted FET element **70**, and the third body-contacted FET element **72** according to one embodiment of the first body-contacted RF switch **92**. In an exemplary embodiment of the first body-contacted RF switch **92**, the insulating material **58** extends completely through the thin-film semiconductor device layer **40** down to the insulating layer **38**, such that the insulating material **58** completely surrounds each of the first body-contacted FET element **46**, the second body-contacted FET element **70**, and the third body-contacted FET element **72**, thereby substantially eliminating conduction paths between the first, the second, and the third body-contacted FET elements **46**, **70**, **72** through the substrate **36**, through the thin-film semiconductor device layer **40**, or both.

FIG. 9 shows a cross-section of the thin-film semiconductor die **34** according to an additional embodiment of the thin-film semiconductor die **34**. The thin-film semiconductor die **34** illustrated in FIG. 9 is similar to the thin-film semiconductor die **34** illustrated in FIG. 8, except that the thin-film semiconductor die **34** illustrated in FIG. 9 further includes the first source contact **64**, the first drain contact **66**, a second source contact **94**, a second drain contact **96**, a third source contact **98**, a third drain contact **100**, a first switch connection node **102**, a second switch connection node **104**, a first FET interconnect **106**, and a second FET interconnect **108**. The contacts **64**, **66**, **94**, **96**, **98**, **100** may be vias that traverse one or more layers of the thin-film semiconductor die **34**. Any or all of the first switch connection node **102**, the second switch connection node **104**, the first FET interconnect **106**, and the second FET interconnect **108** may be provided by one or more metallization layers of the thin-film semiconductor die **34**.

The first source contact **64** is electrically connected to the first source **50**; the first drain contact **66** is electrically connected to the first drain **54**; the second source contact **94** is electrically connected to the second source **76**; the second drain contact **96** is electrically connected to the second drain **80**; the third source contact **98** is electrically connected to the third source **84**; and the third drain contact **100** is electrically connected to the third drain **88**. The first switch connection node **102** of the first body-contacted RF switch **92** is electrically connected to the third source **84** through the third source contact **98**. The second switch connection node **104** of the first body-contacted RF switch **92** is electrically connected to the first drain **54** through the first drain contact **66**. The first FET interconnect **106** electrically connects the first source **50** to the second drain **80** through the first source contact **64** and the second drain contact **96**, respectively. The second FET interconnect **108** electrically connects the second source **76** to the third drain **88** through the second source contact **94** and the third drain contact **100**, respectively. As such, the first body-contacted FET element **46**, the second body-contacted FET element **70**, and the third body-contacted FET element **72** are coupled in series between the first switch connection node **102** and the second switch connection node **104**.

FIG. 10 is a schematic diagram showing the first body-contacted RF switch **92** illustrated in FIG. 9 according to one embodiment of the first body-contacted RF switch **92**. The first body-contacted RF switch **92** includes the first body-contacted FET element **46**, the second body-contacted FET element **70**, the third body-contacted FET element **72**, the first switch connection node **102**, the second switch connection node **104**, a first body bias input FBBI, a first switch control input FSCI, and a resistor bias network **110**. During operation of the first body-contacted RF switch **92**, the first switch control input FSCI may receive a first switch control signal **112** and the first body bias input FBBI may receive a first body bias control signal **114**. The first body-contacted FET element **46**, the second body-contacted FET element **70**, and the third body-contacted FET element **72** are coupled in series between the first switch connection node **102** and the second switch connection node **104**, such that the third source **84** is coupled to the first switch connection node **102**, the third drain **88** is coupled to the second source **76**, the second drain **80** is coupled to the first source **50**, and the first drain **54** is coupled to the second switch connection node **104**.

The resistor bias network **110** is coupled to the first source **50**, the first body **52**, the first drain **54**, the first gate **60**, the second source **76**, the second body **78**, the second drain **80**, the second gate **82**, the third source **84**, the third body **86**, the third drain **88**, the third gate **90**, the first body bias input FBBI, and the first switch control input FSCI. During operation of the first body-contacted RF switch **92**, the resistor bias network **110** may provide appropriate bias behavior to the first source **50**, the first body **52**, the first drain **54**, the first gate **60**, the second source **76**, the second body **78**, the second drain **80**, the second gate **82**, the third source **84**, the third body **86**, the third drain **88**, and the third gate **90** based on the first switch control signal **112**, the first body bias control signal **114**, signals between the first switch connection node **102** and the second switch connection node **104**, or any combination thereof.

FIG. 11 is a schematic diagram showing details of the resistor bias network **110** illustrated in FIG. 10 according to one embodiment of the resistor bias network **110**. The resistor bias network **110** includes a first body bias resistive element RB1, a second body bias resistive element RB2, a third body bias resistive element RB3, a common body bias resistive element RBC, a first gate resistive element RG1, a second gate resistive element RG2, a third gate resistive element RG3, a common gate resistive element RGC, a first drain-to-source resistive element RDS1, a second drain-to-source resistive element RDS2, and a third drain-to-source resistive element RDS3.

The first gate resistive element RG1 is coupled between the first gate **60** and a gate node (not shown) to provide a first gate signal **115** to the first gate **60**. The second gate resistive element RG2 is coupled between the second gate **82** and the gate node to provide a second gate signal **116** to the second gate **82**. The third gate resistive element RG3 is coupled between the third gate **90** and the gate node to provide a third gate signal **118** to the third gate **90**. The common gate resistive element RGC is coupled between the gate node and the first switch control input FSCI. During operation of the first body-contacted RF switch **92**, the first switch control input FSCI may receive the first switch control signal **112**, such that the first, the second, and the third gate signals **115**, **116**, **118** are based on the first switch control signal **112**. The first switch control signal **112** is used to select either the ON state or the OFF state of the first body-contacted RF switch **92**. Selection between the ON state and the OFF state normally occurs at a much lower frequency than the frequency of RF signals

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between the first and the second switch connection nodes **102**, **104**. As such, the first switch control signal **112** may have direct current (DC)-like influences on the first body-contacted RF switch **92**. To minimize the impact of such DC influences, the first, the second, and the third gate resistive elements **RG1**, **RG2**, **RG3** may have large values of resistance to isolate the first, the second, and the third gates **60**, **82**, **90** from one another. Normally, the first body-contacted RF switch **92** will have one of the ON state, the OFF state, or a non-operating state.

The first body bias resistive element **RB1** is coupled between the first body **52** and a body bias node (not shown) to provide a first body bias signal **120** to the first body **52**. The second body bias resistive element **RB2** is coupled between the second body **78** and the body bias node to provide a second body bias signal **122** to the second body **78**. The third body bias resistive element **RB3** is coupled between the third body **86** and the body bias node to provide a third body bias signal **124** to the third body **86**. The common body bias resistive element **RBC** is coupled between the body bias node and the first body bias input **FBBI**. During operation of the first body-contacted RF switch **92**, the first body bias input **FBBI** may receive the first body bias control signal **114**, such that the first, the second, and the third body bias signals **120**, **122**, **124** are based on the first body bias control signal **114**. The first body bias control signal **114** may be used to provide an appropriate body bias to the first, the second, and the third bodies **52**, **78**, **86**, depending on whether the ON state or the OFF state of the first body-contacted RF switch **92** is selected. As mentioned above, selection between the ON state and the OFF state normally occurs at a much lower frequency than the frequency of RF signals between the first and the second switch connection nodes **102**, **104**. Since the first body bias control signal **114** is based on OFF state or ON state selection, the frequency of the first body bias control signal **114** normally occurs at a much lower frequency than the frequency of RF signals between the first and the second switch connection nodes **102**, **104**. As such, the first body bias control signal **114** may have DC like influences on the first body-contacted RF switch **92**. To minimize the impact of such DC influences, the first, the second, and the third body bias resistive elements **RB1**, **RB2**, **RB3** may have large values of resistance to isolate the first, the second, and the third bodies **52**, **78**, **86** from one another.

The first drain-to-source resistive element **RDS1** is coupled between the first drain **54** and the first source **50**, the second drain-to-source resistive element **RDS2** is coupled between the second drain **80** and the second source **76**, and the third drain-to-source resistive element **RDS3** is coupled between the third drain **88** and the third source **84**. During the OFF state, the first, the second, and the third drain-to-source resistive elements **RDS1**, **RDS2**, **RDS3** may provide about equal voltage division across the first, the second, and the third body-contacted FET elements **46**, **70**, **72**.

In a first exemplary embodiment of the first body-contacted RF switch **92**, during the OFF state of the first body-contacted RF switch **92**, a magnitude of the first body bias control signal **114** is about equal to a magnitude of the first switch control signal **112**, and during the ON state of the first body-contacted RF switch **92**, the magnitude of the first body bias control signal **114** is not equal to the magnitude of the first switch control signal **112**.

In a second exemplary embodiment of the first body-contacted RF switch **92**, during the OFF state of the first body-contacted RF switch **92**, the magnitude of the first body bias control signal **114** is about equal to the magnitude of the first switch control signal **112**, the magnitude of the first switch

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control signal **112** is negative relative to a DC voltage at the first switch connection node **102**, and the magnitude of the first switch control signal **112** is negative relative to a DC voltage at the second switch connection node **104**. During the ON state of the first body-contacted RF switch **92**, the magnitude of the first switch control signal **112** is positive relative to the magnitude of the first body bias control signal **114**.

In a third exemplary embodiment of the first body-contacted RF switch **92**, during the OFF state of the first body-contacted RF switch **92**, the magnitude of the first body bias control signal **114** is about equal to the magnitude of the first switch control signal **112**, the magnitude of the first switch control signal **112** is positive relative to the DC voltage at the first switch connection node **102**, and the magnitude of the first switch control signal **112** is positive relative to the DC voltage at the second switch connection node **104**. During the ON state of the first body-contacted RF switch **92**, the magnitude of the first switch control signal **112** is negative relative to the magnitude of the first body bias control signal **114**.

In a fourth exemplary embodiment of the first body-contacted RF switch **92**, during the OFF state of the first body-contacted RF switch **92**, the first body bias control signal **114** is equal to between about -1 volt DC (VDC) and about -5 VDC, the first switch control signal **112** is equal to between about -1 VDC and about -5 VDC, the DC voltage at the first switch connection node **102** is equal to about zero volts, and the DC voltage at the second switch connection node **104** is equal to about zero volts. During the ON state of the first body-contacted RF switch **92**, the first body bias control signal **114** is equal to about zero VDC, the first switch control signal **112** is equal to between about 1 VDC and about 5 VDC, the DC voltage at the first switch connection node **102** is equal to about zero volts, and the DC voltage at the second switch connection node **104** is equal to about zero volts.

During the OFF state of the first body-contacted RF switch **92**, the first body-contacted RF switch **92** has an OFF state impedance between the first and the second switch connection nodes **102**, **104**. During the ON state of the first body-contacted RF switch **92**, the first body-contacted RF switch **92** has an ON state impedance between the first and the second switch connection nodes **102**, **104**. In the illustrated embodiment of the first body-contacted RF switch **92**, the first, the second, and the third body-contacted FET elements **46**, **70**, **72** are coupled in series between the first and the second switch connection nodes **102**, **104**. As such, three body-contacted FET elements are coupled in series. In an alternate embodiment of the first body-contacted RF switch **92**, the second body-contacted FET element **70** is omitted, such that the third drain **88** is directly coupled to the first source **50**. As such, two body-contacted FET elements are coupled in series. In additional embodiments of the first body-contacted RF switch **92**, any number of body-contacted FET elements may be coupled in series.

FIG. **12** is a schematic diagram showing the first body-contacted RF switch **92** according to an alternate embodiment of the first body-contacted RF switch **92**. The first body-contacted RF switch **92** illustrated in FIG. **12** is similar to the first body-contacted RF switch **92** illustrated in FIG. **10**, except the first body-contacted RF switch **92** illustrated in FIG. **12** may include any number of body-contacted FET elements. The first body-contacted RF switch **92** includes the first body-contacted FET element **46**, the second body-contacted FET element **70**, and up to and including an N^{TH} body-contacted FET element **126**. The N^{TH} body-contacted FET element **126** includes an N^{TH} source **128**, an N^{TH} body **130**, an N^{TH} drain **132**, and an N^{TH} gate **134**. The N^{TH} body-contacted FET element **126** and any intervening body-con-

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tacted FET elements (not shown) between the second body-contacted FET element 70 and the N^{TH} body-contacted FET element 126 may be similar to the first body-contacted FET element 46 as previously described.

The first body-contacted FET element 46, the second body-contacted FET element 70, and up to and including the N^{TH} body-contacted FET element 126 are coupled in series between the first switch connection node 102 and the second switch connection node 104, such that the N^{TH} source 128 is coupled to the first switch connection node 102, the N^{TH} drain 132 is coupled to the second source 76 through any intervening body-contacted FET elements (not shown), the second drain 80 is coupled to the first source 50, and the first drain 54 is coupled to the second switch connection node 104. The resistor bias network 110 provides the first gate signal 115 to the first gate 60, the second gate signal 116 to the second gate 82, and an N^{TH} gate signal 136 to the N^{TH} gate 134. During operation of the first body-contacted RF switch 92, the first switch control input FSCI may receive the first switch control signal 112, such that the first, the second, and up to and including the N^{TH} gate signals 115, 116, 136 are based on the first switch control signal 112. The first switch control signal 112 is used to select either the ON state or the OFF state of the first body-contacted RF switch 92.

The resistive bias network 110 provides the first body bias signal 120 to the first body 52, the second body bias signal 122 to the second body 78, and an N^{TH} body bias signal 138 to the N^{TH} body 130. During operation of the first body-contacted RF switch 92, the first body bias input FBBI may receive the first body bias control signal 114, such that the first, the second, and up to and including the N^{TH} body bias signals 120, 122, 138 are based on the first body bias control signal 114. The first body bias control signal 114 may be used to provide an appropriate body bias to the first, the second, and up to and including the N^{TH} bodies 52, 78, 130, depending on whether the ON state or the OFF state of the first body-contacted RF switch 92 is selected.

The first body-contacted RF switch 92 includes a quantity of series coupled body-contacted FET elements equal to N, such that N is any positive whole number greater than one. An RF signal 140 between the first and the second switch connection nodes 102, 104 may be present due to the first body-contacted RF switch 92 interacting with other circuit elements (not shown). In one embodiment of the first body-contacted RF switch 92, a frequency of the RF signal 140 is greater than about 100 megahertz. During the OFF state of the first body-contacted RF switch 92, the RF signal 140 may be distributed across the first body-contacted FET element 46, the second body-contacted FET element 70, and up to and including the N^{TH} body-contacted FET element 126. In an exemplary embodiment of the first body-contacted RF switch 92, during the OFF state of the first body-contacted RF switch 92, the RF signal 140 is distributed about equally across the first body-contacted FET element 46, the second body-contacted FET element 70, and up to and including the N^{TH} body-contacted FET element 126.

FIG. 13 shows an RF switch system 142 according to one embodiment of the RF switch system 142. The RF switch system 142 provides four switched ports and includes the first body-contacted RF switch 92, a second body-contacted RF switch 144, a third body-contacted RF switch 146, a fourth body-contacted RF switch 148, and control circuitry 150. The second, the third, and the fourth body-contacted RF switches 144, 146, 148 may be similar to the first body-contacted RF switch 92. The second body-contacted RF switch 144 has a third switch connection node 152 and a fourth switch connection node 154, which may be similar to the first switch con-

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nection node 102 and the second switch connection node 104, respectively. Further, the second body-contacted RF switch 144 has a second body bias input SBBI and a second switch control input SSCI, which may be similar to the first body bias input FBBI and the first switch control input FSCI, respectively.

The third body-contacted RF switch 146 has a fifth switch connection node 156 and a sixth switch connection node 158, which may be similar to the first switch connection node 102 and the second switch connection node 104, respectively. Further, the third body-contacted RF switch 146 has a third body bias input TBBI and a third switch control input TSCI, which may be similar to the first body bias input FBBI and the first switch control input FSCI, respectively.

The fourth body-contacted RF switch 148 has a seventh switch connection node 160 and an eighth switch connection node 162, which may be similar to the first switch connection node 102 and the second switch connection node 104, respectively. Further, the fourth body-contacted RF switch 148 has a fourth body bias input FOBBI and a fourth switch control input FOSCI, which may be similar to the first body bias input FBBI and the first switch control input FSCI, respectively.

Each of the first, the second, the third, and the fourth body-contacted RF switches 92, 144, 146, 148 provides a switched port of the RF switch system 142. The second, the fourth, the sixth, and the eighth switch connection nodes 104, 154, 158, 162 are coupled to an RF antenna 164. The first, the third, the fifth, and the seventh switch connection nodes 102, 152, 156, 160 provide a first port 166, a second port 168, a third port 170, and a fourth port 172, respectively. Therefore, the first, the second, the third, and the fourth body-contacted RF switches 92, 144, 146, 148 allow the first, the second, the third, and the fourth ports 166, 168, 170, 172 to share the RF antenna 164. Any or all of the first, the second, the third, and the fourth ports 166, 168, 170, 172 may be coupled to RF transmit circuitry (not shown), RF receive circuitry (not shown), RF diplexers (not shown), RF duplexers (not shown), the like (not shown), or any combination thereof (not shown).

The control circuitry 150 provides the first switch control signal 112, a second switch control signal 174, a third switch control signal 176, and a fourth switch control signal 178 to the first switch control input FSCI, the second switch control input SSCI, the third switch control input TSCI, and the fourth switch control input FOSCI, respectively. The control circuitry 150 selects either the OFF state of the first body-contacted RF switch 92 or the ON state of the first body-contacted RF switch 92 and provides the first switch control signal 112 based on the selected one of the OFF state and the ON state to indicate which state was selected. The control circuitry 150 selects either an OFF state of the second body-contacted RF switch 144 or an ON state of the second body-contacted RF switch 144 and provides the second switch control signal 174 based on the selected one of the OFF state and the ON state to indicate which state was selected. The control circuitry 150 selects either an OFF state of the third body-contacted RF switch 146 or an ON state of the third body-contacted RF switch 146 and provides the third switch control signal 176 based on the selected one of the OFF state and the ON state to indicate which state was selected. The control circuitry 150 selects either an OFF state of the fourth body-contacted RF switch 148 or an ON state of the fourth body-contacted RF switch 148 and provides the fourth switch control signal 178 based on the selected one of the OFF state and the ON state to indicate which state was selected.

The control circuitry 150 provides the first body bias control signal 114, a second body bias control signal 180, a third body bias control signal 182, and a fourth body bias control

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signal **184** to the first body bias input FBBI, the second body bias input SBBI, the third body bias input TBBI, and the fourth body bias input FOBBI, respectively. The control circuitry **150** provides the first body bias control signal **114** based on the selected one of the OFF state and the ON state of the first body-contacted RF switch **92** to provide the appropriate body biasing to the body-contacted FET elements (not shown) in the first body-contacted RF switch **92**. The control circuitry **150** provides the second body bias control signal **180** based on the selected one of the OFF state and the ON state of the second body-contacted RF switch **144** to provide the appropriate body biasing to the body-contacted FET elements (not shown) in the second body-contacted RF switch **144**. The control circuitry **150** provides the third body bias control signal **182** based on the selected one of the OFF state and the ON state of the third body-contacted RF switch **146** to provide the appropriate body biasing to the body-contacted FET elements (not shown) in the third body-contacted RF switch **146**. The control circuitry **150** provides the fourth body bias control signal **184** based on the selected one of the OFF state and the ON state of the fourth body-contacted RF switch **148** to provide the appropriate body biasing to the body-contacted FET elements (not shown) in the fourth body-contacted RF switch **148**.

Alternate embodiments of the RF switch system **142** may omit any or all of the second, the third, and the fourth body-contacted RF switches **144**, **146**, **148**, or may include additional body-contacted RF switches (not shown). Further, the body-contacted RF switches may be arranged in any manner.

FIG. **14** shows the RF switch system **142** according to an alternate embodiment of the RF switch system **142**. The RF switch system **142** illustrated in FIG. **14** is similar to the RF switch system **142** illustrated in FIG. **13** except the RF switch system **142** illustrated in FIG. **14** uses the second, the third, and the fourth body-contacted RF switches **144**, **146**, **148** in a different manner. In FIG. **13**, the second, the fourth, the sixth, and the eighth switch connection nodes **104**, **154**, **158**, **162** are coupled to the RF antenna **164**. The first, the third, the fifth, and the seventh switch connection nodes **102**, **152**, **156**, **160** provide the first, the second, the third, and the fourth ports **166**, **168**, **170**, **172**, respectively. In FIG. **14**, the third and the fourth ports **170**, **172** are omitted. The first and the third switch connection nodes **102**, **152** provide the first port **166**, and the fifth and the seventh switch connection nodes **156**, **160** provide the second port **168**. The second and the sixth switch connection nodes **104**, **158** are coupled to the RF antenna **164**, and the fourth and the eighth switch connection nodes **154**, **162** are coupled to ground. As such, the second and the fourth body-contacted RF switches **144**, **148** function as shunt switches.

Normally, when the first body-contacted RF switch **92** is in the OFF state, the second body-contacted RF switch **144** is in the ON state and vice versa. By coupling the first switch connection node **102** to ground when the first body-contacted RF switch **92** is in the OFF state and the second body-contacted RF switch **144** is in the ON state may improve isolation characteristics of the first body-contacted RF switch **92**. Similarly, normally, when the third body-contacted RF switch **146** is in the OFF state, the fourth body-contacted RF switch **148** is in the ON state and vice versa. By coupling the fifth switch connection node **156** to ground when the third body-contacted RF switch **146** is in the OFF state and the fourth body-contacted RF switch **148** is in the ON state may improve isolation characteristics of the third body-contacted RF switch **146**. Alternate embodiments of the RF switch system **142** may omit any or all of the second, the third, and the fourth body-contacted RF switches **144**, **146**, **148**, or may include

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additional body-contacted RF switches (not shown). Further, the body-contacted RF switches may be arranged in any manner.

An application example of the RF switch system **142** is its use in a mobile terminal **186**, the basic architecture of which is represented in FIG. **15**. The mobile terminal **186** may include a receiver front end **188**, a radio frequency transmitter section **190**, an antenna **192**, the RF switch system **142**, a baseband processor **194**, a control system **196**, a frequency synthesizer **198**, and an interface **200**. The receiver front end **188** receives information bearing radio frequency signals from one or more remote transmitters provided by a base station (not shown). A low noise amplifier (LNA) **202** amplifies the signal. A filter circuit **204** minimizes broadband interference in the received signal, while down conversion and digitization circuitry **206** down converts the filtered, received signal to an intermediate or baseband frequency signal, which is then digitized into one or more digital streams. The receiver front end **188** typically uses one or more mixing frequencies generated by the frequency synthesizer **198**. The baseband processor **194** processes the digitized received signal to extract the information or data bits conveyed in the received signal. This processing typically comprises demodulation, decoding, and error correction operations. As such, the baseband processor **194** is generally implemented in one or more digital signal processors (DSPs).

On the transmit side, the baseband processor **194** receives digitized data, which may represent voice, data, or control information, from the control system **196**, which it encodes for transmission. The encoded data is output to the transmitter **190**, where it is used by a modulator **208** to modulate a carrier signal that is at a desired transmit frequency. Power amplifier circuitry **210** amplifies the modulated carrier signal to a level appropriate for transmission, and delivers the amplified and modulated carrier signal to the antenna **192** through the RF switch system **142**.

A user may interact with the mobile terminal **186** via the interface **200**, which may include interface circuitry **212** associated with a microphone **214**, a speaker **216**, a keypad **218**, and a display **220**. The interface circuitry **212** typically includes analog-to-digital converters, digital-to-analog converters, amplifiers, and the like. Additionally, it may include a voice encoder/decoder, in which case it may communicate directly with the baseband processor **194**. The microphone **214** will typically convert audio input, such as the user's voice, into an electrical signal, which is then digitized and passed directly or indirectly to the baseband processor **194**. Audio information encoded in the received signal is recovered by the baseband processor **194**, and converted by the interface circuitry **212** into an analog signal suitable for driving the speaker **216**. The keypad **218** and display **220** enable the user to interact with the mobile terminal **186**, input numbers to be dialed, address book information, or the like, as well as monitor call progress information.

FIG. **16** is a graph illustrating a relationship between a body-contacted RF switch OFF capacitance of the first body-contacted RF switch **92** (FIGS. **13** and **14**) and an absolute value of reverse body biasing of the first body-contacted RF switch **92**. The body-contacted RF switch OFF capacitance is between the first and the second switch connection nodes **102**, **104** (FIGS. **13** and **14**) when the first body-contacted RF switch **92** is in an OFF state. As mentioned above, reverse body biasing each FET element, which is in an OFF state, in the first body-contacted RF switch **92** may reduce drain-to-source capacitance of each FET element. Since the FET elements are coupled in series, the body-contacted RF switch OFF capacitance may be reduced by the reverse body biasing.

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FIG. 16 shows that as the absolute value of the reverse body biasing increases, the body-contacted RF switch OFF capacitance decreases, which may effectively increase RF isolation of the first body-contacted RF switch 92. The insertion loss of the first body-contacted RF switch 92 may be similar to the insertion loss of a similarly constructed floating-body RF switch. Therefore, reverse body biasing may improve the trade-off between insertion loss and RF isolation.

Additionally, reverse body biasing may improve the linearity of the first body-contacted RF switch 92 by operating where the slope of the capacitance versus the reverse body biasing curve illustrated in FIG. 16 is shallow instead of steep. Linearity of an RF switch is provided by maintaining a constant RF switch OFF capacitance over changes in magnitudes of RF signal levels across the RF switch. RF signals across an RF switch modulate the body biasing of the RF switch. However, modulating body biasing modulates the RF switch OFF capacitance as illustrated in FIG. 16. As magnitudes of the RF signals increase, magnitudes of the modulations increase, thereby causing non-linearity in the RF switch 92. Further, by examining the shape of the curve illustrated in FIG. 16, when the absolute value of reverse body biasing is close to zero, the slope of the curve is steep, thereby causing large modulations of the RF switch OFF capacitance due to modulations of the body biasing. Such large modulations of the RF switch OFF capacitance may cause significant non-linearity in the RF switch. However, when the absolute value of reverse body biasing is large, the slope of the curve is shallow, thereby reducing modulations of the RF switch OFF capacitance due to modulations of the body biasing. Such reduced modulations of the body-contacted RF switch OFF capacitance may significantly improve linearity in the first body-contacted RF switch 92.

FIG. 17 is a graph illustrating a relationship between second harmonic power of both floating-body and body-contacted RF switches in an OFF state and input power to the RF switches. Further, FIG. 18 is a graph illustrating a relationship between third harmonic power of both floating-body and body-contacted RF switches in an OFF state and input power to the RF switches. Harmonic power may be one measure of harmonic distortion, which may degrade the linearity of the first body-contacted RF switch 92 (FIGS. 13 and 14). Harmonic distortion may be caused by changes in the body-contacted RF switch OFF capacitance resulting from the time-varying nature of RF signals between the first and the second switch connection nodes 102, 104 of the first body-contacted RF switch 92. As mentioned above, the body-contacted RF switch OFF capacitance may result from capacitances of series-coupled FET elements in the first body-contacted RF switch 92. Each FET element may have a drain-to-body capacitance, a drain-to-gate capacitance, and a drain-to-source capacitance. By applying reverse body biasing, the drain-to-body capacitance may be reduced and may have a reduced sensitivity to changes in input power, when compared to a floating-body RF switch. As a result, as illustrated in FIG. 17, the second harmonic power of the first body-contacted RF switch 92 is slightly less than corresponding second harmonic power of the floating-body RF switch. However, as illustrated in FIG. 18, the third harmonic power of the first body-contacted RF switch 92 is significantly less than the third harmonic power of the floating-body RF switch, particularly as input power increases.

FIG. 19 shows a top view of details of the first body-contacted FET element 46 illustrated in FIG. 4 according to one embodiment of the first body-contacted FET element 46. The first body-contacted FET element 46 illustrated in FIG. 19 is similar to the first body-contacted FET element 46

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illustrated in FIG. 7, except in the first body-contacted FET element 46 illustrated in FIG. 19, the first gate 60 has multiple gate fingers 222, the first source 50 has multiple source fingers 224, and the first drain 54 has multiple drain fingers 226. Each of the multiple gate fingers 222 may be between one of the multiple source fingers 224 and one of the multiple drain fingers 226. Further, each of the multiple source fingers 224 may have at least one of the first source contacts 64. Similarly, each of the multiple drain fingers 226 may have at least one of the first drain contacts 66. Other embodiments of the first body-contacted FET element 46 may have any arrangement of the first gate 60, the first drain 54, and the first source 50 including any number of source fingers 224, drain fingers 226, and gate fingers 222.

FIG. 20 shows a top view of details of the first body-contacted FET element 46 illustrated in FIG. 4 according to an alternate embodiment of the first body-contacted FET element 46. The first body-contacted FET element 46 illustrated in FIG. 20 is similar to the first body-contacted FET element 46 illustrated in FIG. 19, except in the first body-contacted FET element 46 illustrated in FIG. 20, the multiple gate fingers 222 are coupled together at both ends instead of only at one end as illustrated in FIG. 19. Further, both ends of the first gate 60 may have at least one first gate contact 62.

Some of the circuitry previously described may use discrete circuitry, integrated circuitry, programmable circuitry, non-volatile circuitry, volatile circuitry, software executing instructions on computing hardware, firmware executing instructions on computing hardware, the like, or any combination thereof. The computing hardware may include mainframes, micro-processors, micro-controllers, DSPs, the like, or any combination thereof.

None of the embodiments of the present disclosure are intended to limit the scope of any other embodiment of the present disclosure. Any or all of any embodiment of the present disclosure may be combined with any or all of any other embodiment of the present disclosure to create new embodiments of the present disclosure.

Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

What is claimed is:

1. A semiconductor die comprising:

an insulating layer;

a thin-film semiconductor device layer over the insulating layer;

a first body-contacted radio frequency (RF) switch having one of an ON state and an OFF state, and a non-operating state and comprising a first plurality of body-contacted field effect transistor (FET) elements coupled in series, such that each body-contacted FET element comprises a source, a drain, and a body formed in at least a part of the thin-film semiconductor device layer, wherein each one of the first plurality of body-contacted FET elements are separated from one another in the thin-film semiconductor device layer by an insulating material; and

control circuitry coupled to each one of the first plurality of body-contacted FET elements, wherein during the OFF state of the first body-contacted RF switch, the control circuitry provides each body a body bias signal, such that each body and each corresponding source are reverse biased and each body and each corresponding drain are reverse biased to provide reverse body biasing of each corresponding body-contacted FET element.

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2. The semiconductor die of claim 1 wherein:
the control circuitry is further adapted to:
select the OFF state of the first body-contacted RF switch; and
provide a first body bias control signal, such that each body bias signal is based on the first body bias control signal.
3. The semiconductor die of claim 2 wherein the first body-contacted RF switch further comprises:
a first body bias input adapted to receive the first body bias control signal; and
a resistor bias network comprising a plurality of body bias resistive elements, such that each of at least some of the plurality of body bias resistive elements is coupled between a body of a corresponding one of the first plurality of body-contacted FET elements and the first body bias input.
4. The semiconductor die of claim 3 wherein:
the control circuitry is further adapted to provide a first switch control signal based on one of the OFF state and the ON state;
the first body-contacted RF switch further comprises a first switch connection node and a second switch connection node, such that all of the first plurality of body-contacted FET elements are coupled in series between the first switch connection node and the second switch connection node;
during the OFF state, the first body-contacted RF switch has an OFF state impedance between the first switch connection node and the second switch connection node; and
during the ON state, the first body-contacted RF switch has an ON state impedance between the first switch connection node and the second switch connection node.
5. The semiconductor die of claim 4 wherein:
the first body-contacted RF switch further comprises a first switch control input adapted to receive the first switch control signal; and
each of the first plurality of body-contacted FET elements further comprises a gate, which is coupled to the first switch control input.
6. The semiconductor die of claim 5 wherein the resistor bias network further comprises a plurality of gate resistive elements, such that each of at least some of the plurality of gate resistive elements is coupled between the gate of a corresponding one of the first plurality of body-contacted FET elements and the first switch control input.
7. The semiconductor die of claim 6 wherein:
during the OFF state:
the first switch connection node has a direct current (DC) voltage equal to about zero volts;
the second switch connection node has a DC voltage equal to about zero volts;
the first body bias control signal is equal to between about -1 volt DC (VDC) and about -5VDC; and
the first switch control signal is equal to between about -1VDC and about -5VDC; and
during the ON state:
the first switch connection node has a DC voltage equal to about zero volts;
the second switch connection node has a DC voltage equal to about zero volts;
the first body bias control signal is equal to about zero volts; and
the first switch control signal is equal to between about 1VDC and about 5VDC.

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8. The semiconductor die of claim 1 wherein a thickness of the thin-film semiconductor device layer is less than about 500 nanometers.
9. The semiconductor die of claim 8 wherein a thickness of the insulating layer is greater than the thickness of the thin-film semiconductor device layer.
10. The semiconductor die of claim 9 wherein the thickness of the thin-film semiconductor device layer is between about 100 nanometers and about 300 nanometers and the thickness of the insulating layer is between about 200 nanometers and about 1000 nanometers.
11. The semiconductor die of claim 9 further comprising a substrate, such that the insulating layer is over the substrate, and a resistivity of the substrate is greater than about 100 ohm-centimeters.
12. The semiconductor die of claim 1 wherein the source of each of the first plurality of body-contacted FET elements and the drain of each of the first plurality of body-contacted FET elements completely traverse a thickness of the thin-film semiconductor device layer.
13. The semiconductor die of claim 12 wherein:
the source of each of the first plurality of body-contacted FET elements comprises N-type silicon;
the drain of each of the first plurality of body-contacted FET elements comprises N-type silicon; and
the body of each of the first plurality of body-contacted FET elements comprises P-type silicon.
14. The semiconductor die of claim 12 wherein:
the source of each of the first plurality of body-contacted FET elements comprises P-type silicon;
the drain of each of the first plurality of body-contacted FET elements comprises P-type silicon; and
the body of each of the first plurality of body-contacted FET elements comprises N-type silicon.
15. The semiconductor die of claim 1 wherein the first body-contacted RF switch further comprises a first switch connection node and a second switch connection node, such that:
all of the first plurality of body-contacted FET elements are coupled in series between the first switch connection node and the second switch connection node; and
during the OFF state of the first body-contacted RF switch, an RF signal between the first switch connection node and the second switch connection node is distributed across the first plurality of body-contacted FET elements.
16. The semiconductor die of claim 15 wherein a frequency of the RF signal is greater than about 100 megahertz.
17. The semiconductor die of claim 16 wherein during the OFF state of the first body-contacted RF switch, the RF signal between the first switch connection node and the second switch connection node is distributed about equally across the first plurality of body-contacted FET elements.
18. The semiconductor die of claim 1 further comprising a substrate wherein:
the insulating layer is over the substrate; and
the insulating layer substantially eliminates conduction paths through the substrate to the other devices.
19. The semiconductor die of claim 1 wherein the thin-film semiconductor device layer is partially-depleted and not fully-depleted.
20. The semiconductor die of claim 1 further comprising a second body-contacted RF switch coupled between the first body-contacted RF switch and ground.
21. The semiconductor die of claim 1 wherein the thin-film semiconductor device layer comprises silicon.

22. The semiconductor die of claim **21** further comprising a silicon-on-insulator (SOI) substrate, such that:

the semiconductor die is an SOI semiconductor die;
the insulating layer is an SOI insulating layer, which is over the SOI substrate; and
the thin-film semiconductor device layer is a thin-film SOI device layer.

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23. The semiconductor die of claim **1** wherein the insulating layer provides a substrate of the semiconductor die.

24. The semiconductor die of claim **23** wherein the insulating layer comprises sapphire.

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25. The semiconductor die of claim **1** further comprising a plurality of drain-to-source resistive elements, such that each of the plurality of drain-to-source resistive elements is coupled between a corresponding drain and a corresponding source of the first plurality of body-contacted FET elements.

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